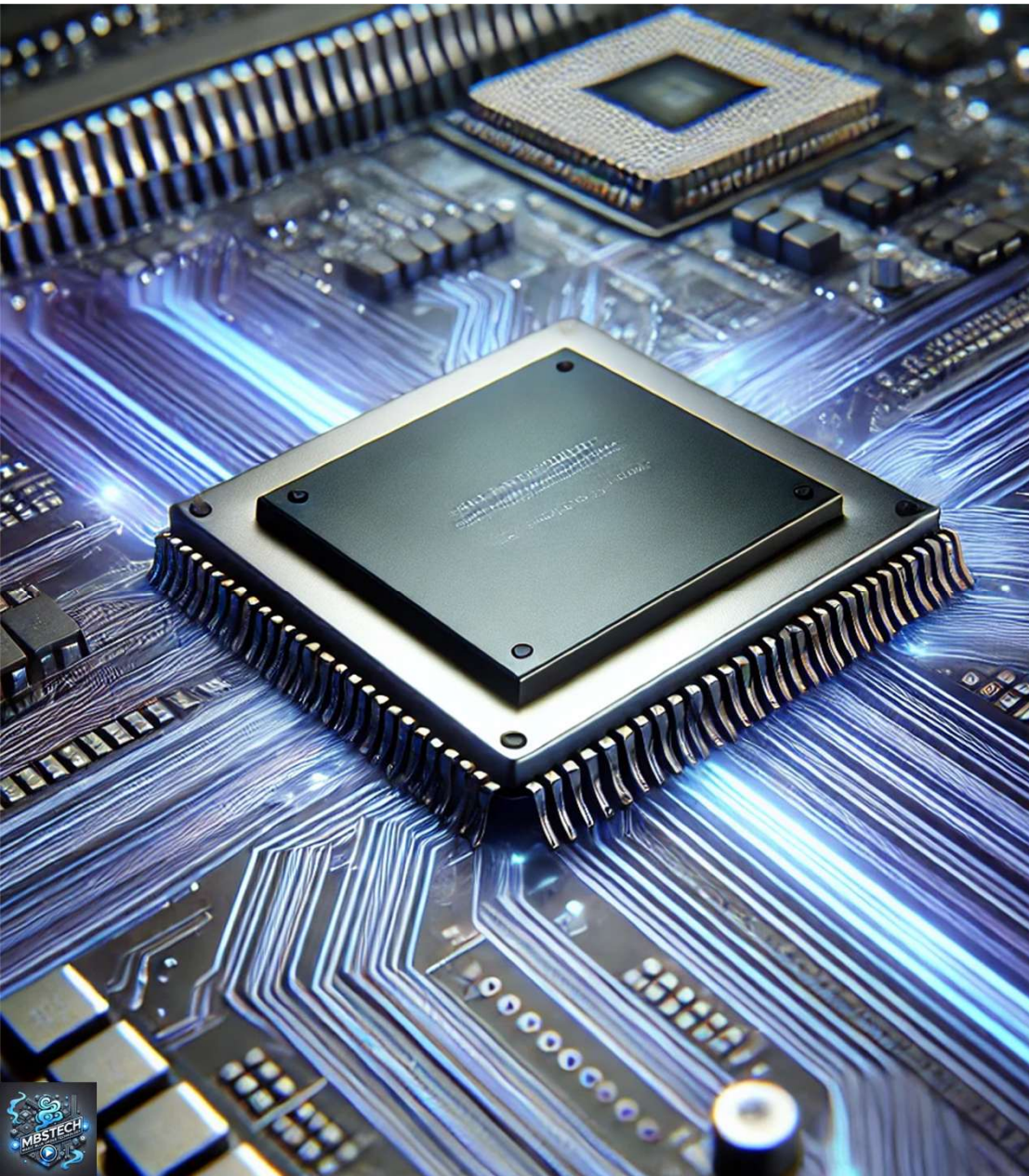

S.I AND P.I CHALLENGES IN FPGA'S

Introduction

Field Programmable Gate Arrays (FPGAs) are essential components in modern embedded and aerospace systems, providing flexibility, performance, and scalability. However, as FPGA architectures become more complex and operate at higher speeds, maintaining signal integrity (SI) and power integrity (PI) is increasingly challenging. Poor SI/PI design can lead to degraded performance, increased electromagnetic interference (EMI), data corruption, and even system failures. This presentation explores key challenges and best practices for ensuring robust SI/PI in FPGA-based designs, with a specific focus on Microsemi IGLOO2 and PolarFire FPGAs.

Power Point Presentation By
Andy Carpenter 2025





POWER INTEGRITY IN FPGA DESIGNS

- Ensuring power integrity in FPGA-based designs is critical to maintaining stable operation and high performance. Power integrity issues, such as voltage fluctuations, excessive noise, and inadequate current delivery, can lead to timing errors, reduced reliability, and system instability. As FPGA devices incorporate more transceivers, processors, and high-speed interfaces, their power demands become more dynamic, requiring careful design considerations in the power delivery network (PDN). This section explores key power integrity challenges and best practices for optimizing PDN design, mitigating noise, and ensuring a stable power supply for FPGAs.

POWER INTEGRITY IN FPGA DESIGNS CONT...

Introduction

The Power Delivery Network (PDN) is a critical component in FPGA designs, ensuring stable and reliable power distribution to all system components. An optimized PDN minimizes impedance, reduces noise, and prevents voltage fluctuations that can impact FPGA performance. As modern FPGAs demand higher power at different voltage levels, careful planning of the PDN is essential to support dynamic current loads and minimize power integrity issues. Some of these topics are shown to the right...

Establishing a Power Delivery Network (PDN)

- **Designing a Low Impedance Power Distribution Network**
- **Voltage Ripple and Transients**
- **Selecting and Placing Decoupling Capacitors**
- **Minimising Ground Bounce and Power Supply Noise**
- **Optimising PCB Stack up for Power Integrity**



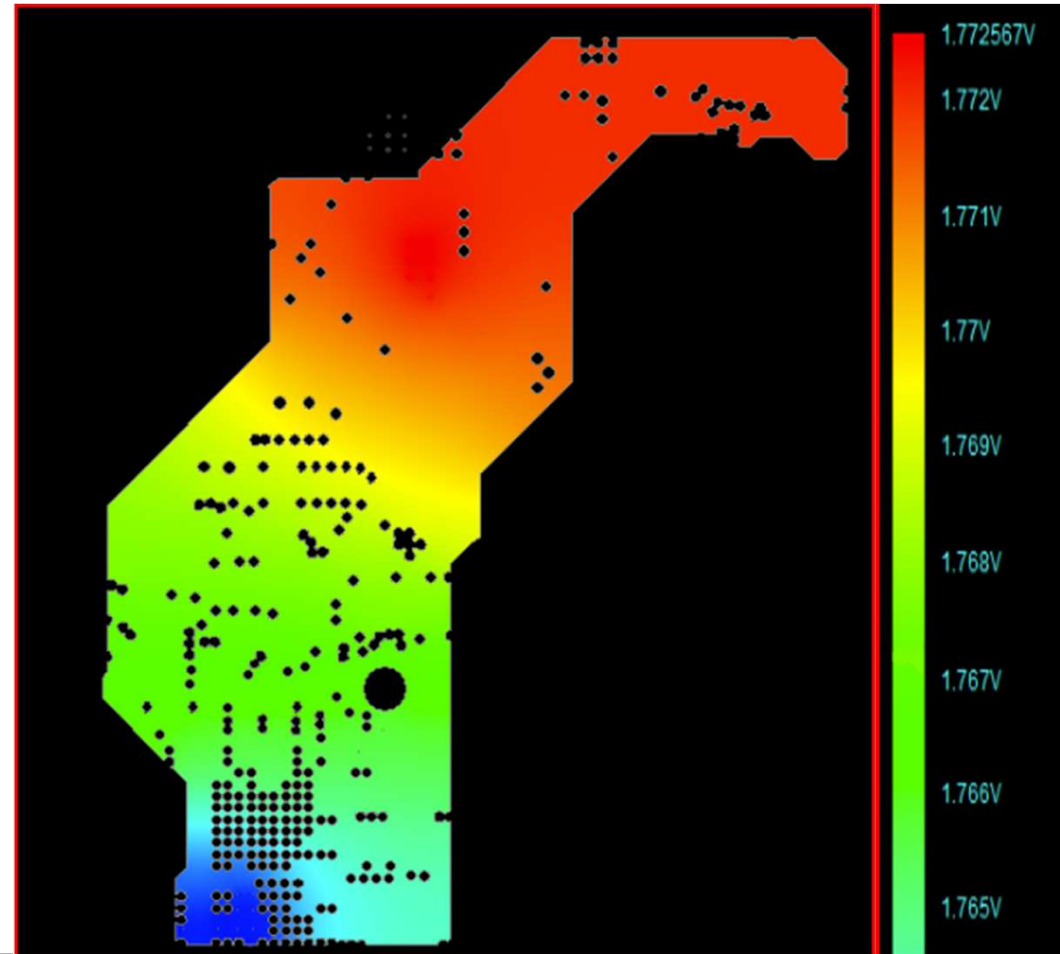
DESIGNING A LOW IMPEDANCE POWER DISTRIBUTION NETWORK

Introduction

Designing a low impedance power distribution network (PDN) is critical for ensuring stable voltage levels and mitigating power integrity issues in FPGA-based systems. A low-impedance PDN minimizes voltage fluctuations, reduces noise, and improves transient response, ensuring reliable FPGA operation under varying load conditions. The goal is to create a robust power delivery path from the voltage regulator module (VRM) to the FPGA while minimizing parasitic inductance and resistance.

The image is an example of a PDN simulation output, showing voltage drops from source to load.

Some of the things to consider are...



DESIGNING A LOW IMPEDANCE POWER DISTRIBUTION NETWORK BEST PRACTICE & TIPS

•Minimizing Impedance from VRM to FPGA

- Ensuring a low-resistance pathway is crucial for minimizing DC voltage drop.
- Utilizing wide and short power traces helps to decrease impedance.
- Choosing the right copper thickness is essential for achieving low-resistance power planes.

•Reducing Power Rail Fluctuations and Supply Noise

- Incorporating multiple decoupling capacitors aids in stabilizing voltage levels.
- Employing ferrite beads can effectively filter out high-frequency noise present in power traces.
- Implementing proper grounding methods is necessary to decrease loop inductance.

•Optimizing Via Placement for Current Distribution

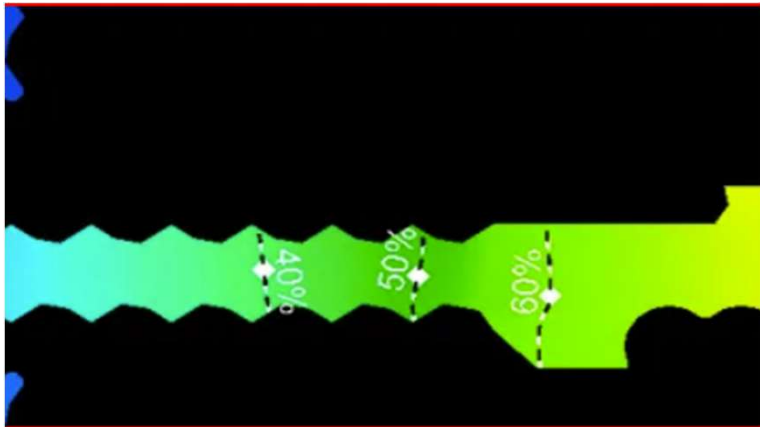
- Careful placement of vias allows for even current distribution.
- Avoiding single-point connections is important to prevent current flow bottlenecks.
- Utilizing multiple vias for both power and ground connections reduces impedance significantly.

•Utilizing Power Plane Segmentation and Stitching

- Creating isolated power regions is beneficial for high-current FPGA blocks.
- Stitching vias across layers helps maintain consistent impedance.
- Optimizing plane design is vital to prevent ground bounce and noise coupling.
- Minimizing impedance between the voltage regulator module (VRM) and the FPGA is of great importance.
- Adopting strategies to reduce fluctuations in power rails and supply noise is essential.

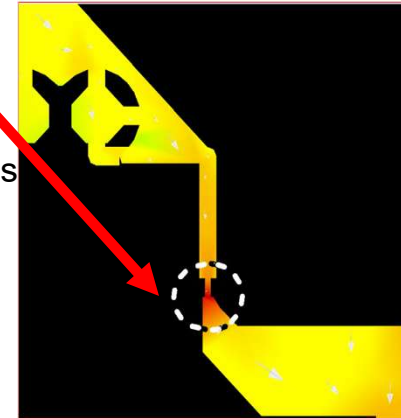


DESIGNING A LOW IMPEDANCE POWER DISTRIBUTION NETWORK BEST PRACTICE & TIPS



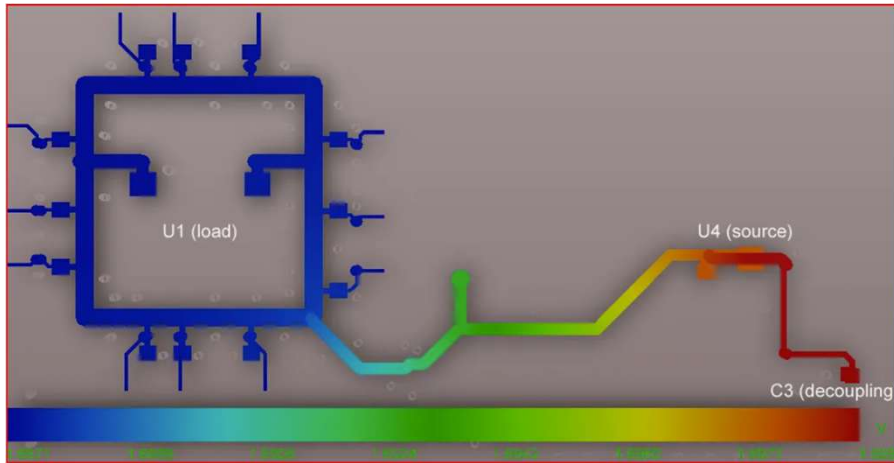
- Power integrity (PI) simulations play a crucial role in the design and verification of high-speed FPGA-based systems. Tools like **CST Studio Suite** (CST PI Solver) provide detailed analysis of power delivery networks (PDN), helping engineers optimize designs before manufacturing. The key benefits include:

- Predicting and Mitigating Voltage Drops
- Resonance and Impedance Optimization
- Identifying Ground and Supply Bounce Issues
- Optimizing Decoupling Strategies
- EMI and Noise Reduction
- Cost and Time Savings



Using PI simulation tools like **CST Analyzer**, engineers can achieve a **robust, low-noise power delivery network** for FPGA-based designs. These simulations enable precise optimization of PCB layouts, power planes, and decoupling strategies, leading to improved reliability, better signal integrity, and reduced EMI challenges.

DESIGNING A LOW IMPEDANCE POWER DISTRIBUTION NETWORK BEST PRACTICE & TIPS



Images courtesy of CST used for education

Poor Example of PDN supplying an IC.

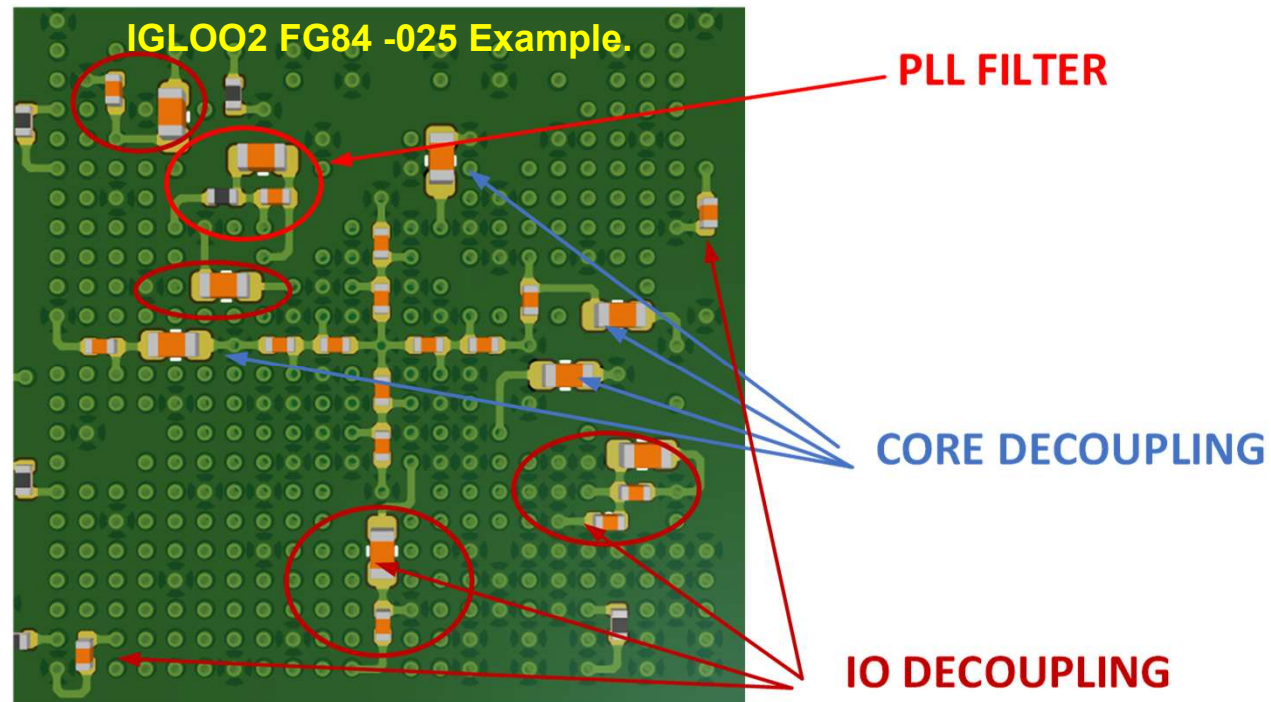
This diagram provides a **color-mapped visualization** of the voltage distribution across a **power delivery network (PDN)**. It highlights how voltage propagates from the **source (U4)** through the PCB traces to the **load (U1)**, with **C3 serving as a decoupling capacitor**.

- The **red region (high voltage)** near **U4 (source)** gradually shifts to **blue (low voltage)** near **U1 (load)**, illustrating the **voltage drop along the PDN path**.
- This suggests a **significant IR drop**, which could impact power integrity, especially for high-speed FPGA designs.
- This is not a good design, but you see it far too often.
- One of the main issues that you see this, is that engineers are not using the more advanced simulation tools which would point out these early issues.
- Quick fixes would be change u4 to a POL source.
- Added more local decoupling
- Thicken up traces, or better still use planes.

SELECTING AND PLACING DECOUPLING CAPACITORS

Introduction

- Decoupling capacitors are essential for stabilizing the power supply and reducing noise in FPGA designs. They help smooth voltage fluctuations, supply transient currents, and filter high-frequency noise, ensuring consistent power delivery to FPGA components. Proper selection and placement of decoupling capacitors are crucial for optimizing power integrity and minimizing impedance variations.
- The image show a BGA with only through hole via's, higher performance lower inductance could be obtained with blind and buried technology.
- Some more thing's to consider are...



SELECTING AND PLACING DECOUPLING CAPACITORS BEST PRACTICE & TIPS



•Choosing Capacitors Across Different Frequency Ranges

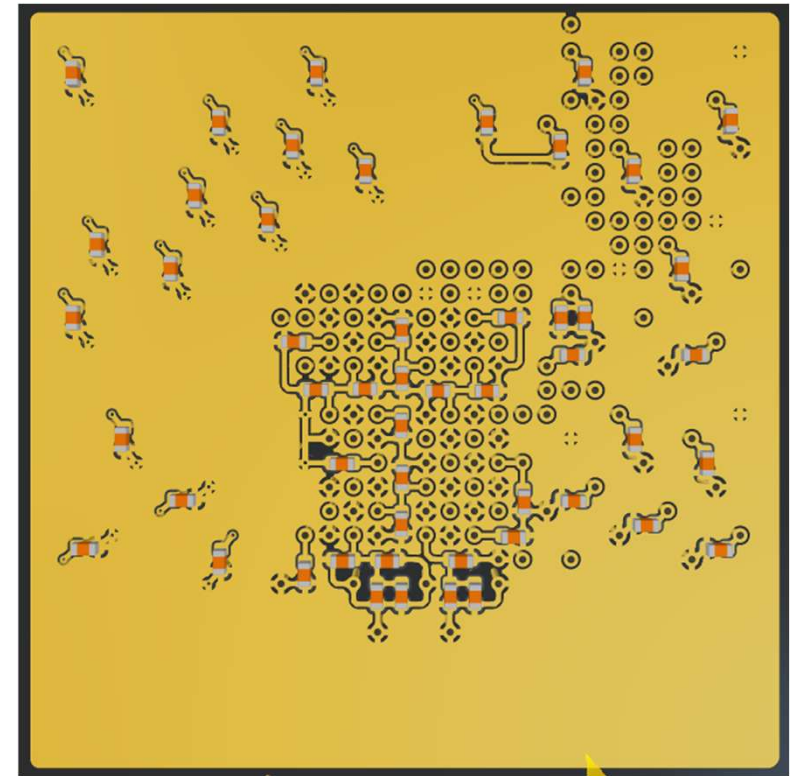
- High-frequency ceramic capacitors (e.g., $0.1\mu\text{F}$, 1nF) for rapid transient response.
- Mid-range capacitors (e.g., $1\mu\text{F}$, $10\mu\text{F}$) for handling intermediate noise filtering.
- Bulk capacitors (e.g., $100\mu\text{F}$, $470\mu\text{F}$) to stabilize power supply over longer durations.

•Guidelines for Optimal Capacitor Placement

- Placing capacitors as close as possible to FPGA power pins to minimize loop inductance.
- Distributing capacitors evenly across the PCB to prevent localized power dips.
- Using via arrays to connect capacitors to power planes for low-impedance paths.

•Minimizing Parasitic Effects

- Reducing lead and trace inductance by using short, wide traces.
- Using multiple ground vias to improve capacitor effectiveness.
- Avoiding excessive capacitor stacking, which can introduce resonance effects.

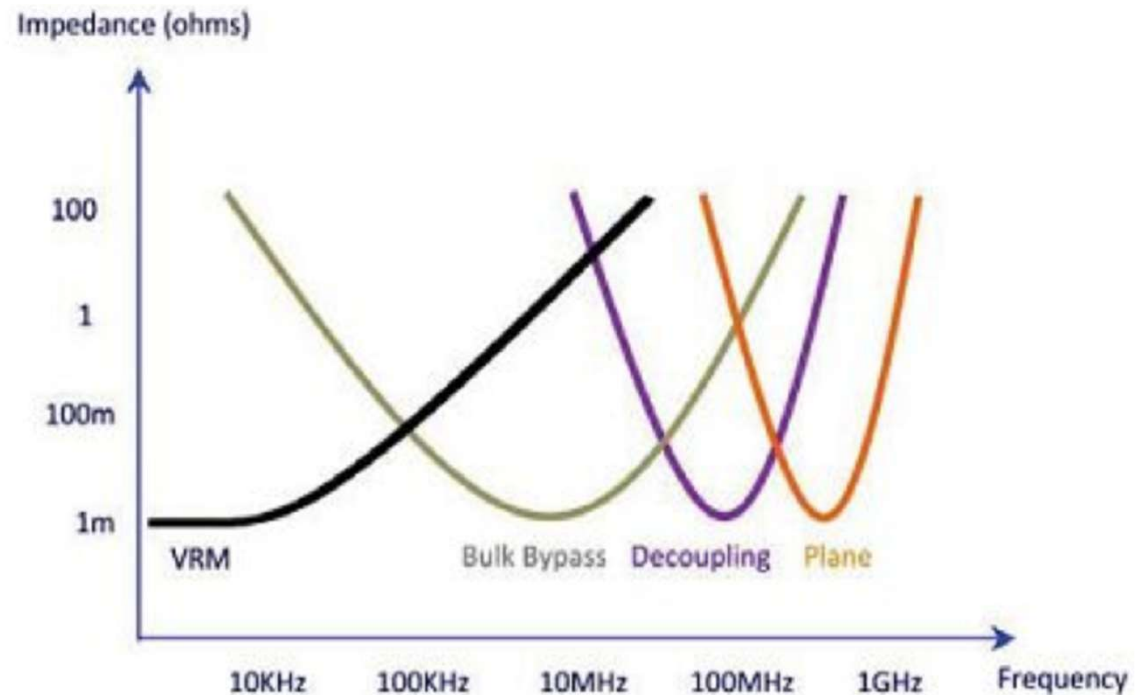


SELECTING AND PLACING DECOUPLING CAPACITORS BEST PRACTICE & TIPS



Simulation and Measurement Techniques

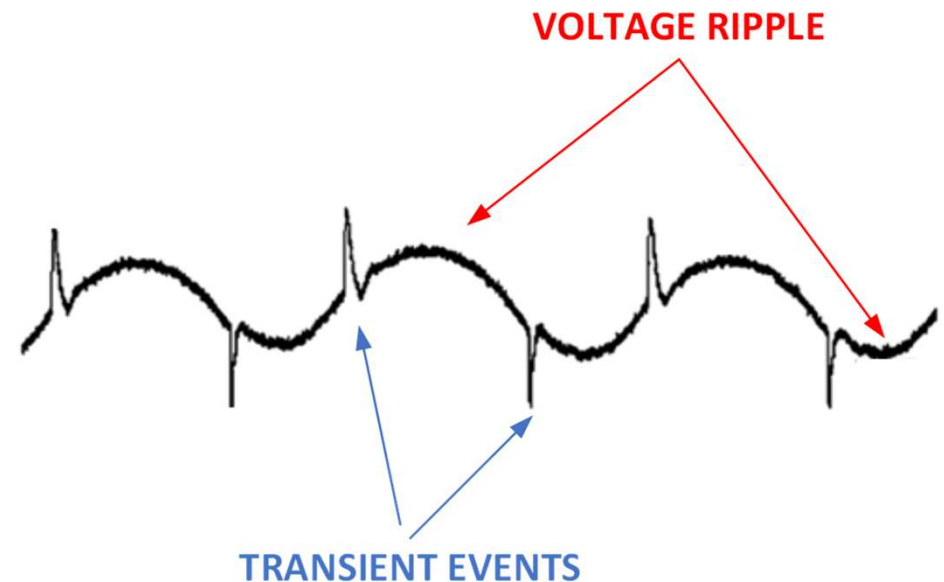
- Using SPICE simulations to model capacitor response under different loads.
- Measuring capacitor effectiveness with impedance analyzers and oscilloscopes, whilst ensuring proper performance through pre-layout and post-layout validation.
- Choose capacitors across different frequency ranges to address transient currents.
- Follow guidelines for optimal capacitor placement to minimize power delivery impedance.



VOLTAGE RIPPLE AND TRANSIENTS

Introduction

Voltage ripple and transients pose a significant challenge in FPGA power integrity, affecting performance and stability. These fluctuations arise due to sudden changes in current demand, improper capacitor selection, and inadequate voltage regulation. Managing voltage ripple involves careful PDN design, proper selection of decoupling capacitors, and ensuring a low-impedance power path to minimize unwanted variations in supply voltage. Some of the things to consider are...



VOLTAGE RIPPLE AND TRANSIENTS BEST PRACTICE & TIPS



- **Considerations for PCB Design to Minimise Voltage Ripple**
 - Optimising the widths of power traces and reducing resistance.
 - Ensuring a low-impedance return path for transient currents.
 - **Techniques for Simulation and Measurement**
 - Employing SPICE simulations to model transient behaviour.
 - Measuring voltage ripple using oscilloscopes and frequency analysers.
 - Simulating and selecting the voltage regulator module (VRM) to ensure low-noise operations while injecting load transients and assessing the effect on FPGA performance.
 - Performing PDN simulations to determine the optimal placement of bulk capacitors for enhancing transient response.
 - **Understanding Load Transients**
 - Rapid current demand changes due to FPGA switching activities.
 - Effects of transient loads on voltage stability and performance.
 - **Voltage Regulator Module (VRM) Selection**
 - Choosing low-noise VRMs to minimize ripple effects.
 - Impact of regulator response time on transient voltage deviations.
 - **Bulk and High-Frequency Capacitor Placement**
 - Role of bulk capacitors in stabilizing large transient currents.
 - Importance of high-frequency decoupling capacitors in reducing ripple.
-



POWER INTEGRITY IN FPGA DESIGNS CONT...

Introduction

Voltage ripple and transients pose a significant challenge in FPGA power integrity, affecting performance and stability. These fluctuations arise due to sudden changes in current demand, improper capacitor selection, and inadequate voltage regulation. Managing voltage ripple involves careful PDN design, proper selection of decoupling capacitors, and ensuring a low-impedance power path to minimize unwanted variations in supply voltage. Some of these topics are shown to the right...

Voltage Ripple & Transients

- Understanding Load Transients
- Voltage Regulator Module (VRM) Selection
- Bulk and High-Frequency Capacitor Placement
- PCB Design Considerations for Reducing Voltage Ripple
- Simulation and Measurement Techniques



POWER INTEGRITY IN FPGA DESIGNS CONT...

Introduction

Modern FPGAs operate with highly dynamic workloads, resulting in rapidly changing current demands. High-speed transceivers, memory interfaces, and logic cores contribute to large transient currents that can cause voltage dips and power instability. Proper power distribution planning, transient response optimization, and decoupling strategies are essential to accommodate these fluctuations and ensure reliable FPGA operation. Some of these topics are shown to the right...

Dynamic Current Demands

- FPGA Power Consumption Variations
- Simultaneous Switching Noise (SSN) and Power Rails
- Transient Current Fluctuations and Compensation
- Power Delivery Network (PDN) Optimization for Dynamic Loads
- Measurement and Simulation Techniques



POWER INTEGRITY IN FPGA DESIGNS CONT...

Introduction

Decoupling capacitors play a crucial role in stabilizing power delivery by filtering noise and supplying instantaneous current demands. A well-designed decoupling strategy balances capacitor selection, placement, and distribution across the PCB to minimize loop inductance and effectively suppress voltage fluctuations. Understanding the interaction of high-frequency and bulk capacitors is key to achieving optimal power integrity in FPGA designs. Some of these topics are shown to the right...

Decoupling Strategies

- Fundamentals of Decoupling
- Optimal Capacitor Placement for Different Frequency Ranges
- High-Frequency vs. Bulk Capacitors: Selecting the Right Mix
- Minimizing Loop Inductance for Effective Noise Suppression
- PCB Design Considerations for Decoupling Optimization
- Simulation and Measurement Techniques



POWER INTEGRITY IN FPGA DESIGNS CONT...

Introduction

Power integrity is closely linked to thermal management in FPGA designs. Excessive power dissipation can lead to overheating, increased resistance, and voltage instability. Efficient heat dissipation techniques, such as thermal vias, heat sinks, and proper PCB design, help maintain consistent power delivery. Monitoring temperature variations and simulating thermal effects are crucial for optimizing power integrity and preventing failures in high-performance FPGA applications. . Some of these topics are shown to the right...

Thermal Implications on Power Integrity

- Power Dissipation Challenges in Dense FPGA Designs
- Role of Heat Sinks, Thermal Vias, and Copper Pours
- Impact of Temperature Variations on Power Delivery
- Thermal Simulation Tools for Assessing FPGA Power Integrity
- Best Practices for Thermal Management in FPGA-Based Systems



MINIMISING GROUND BOUNCE AND POWER SUPPLY NOISE

- **Introduction**

- Ground bounce occurs when multiple FPGA I/Os switch simultaneously, causing transient voltage differences between the IC ground and PCB ground. This results from inductance in the package and PCB, leading to signal integrity issues like false triggering and timing violations.
- Power supply noise, on the other hand, arises from rapid current transients that create voltage fluctuations on power rails. Poor decoupling, inadequate power planes, and excessive IR drops can exacerbate these issues. Both ground bounce and power noise are critical concerns in high-speed FPGA designs, especially for interfaces like DDR, PCIe, and SerDes, where signal stability is essential for reliable operation.

- **Summary**

- **Ground Bounce:**

A transient voltage difference between the IC ground and the PCB ground due to rapid switching of multiple I/Os.

- **Power Supply Noise:**

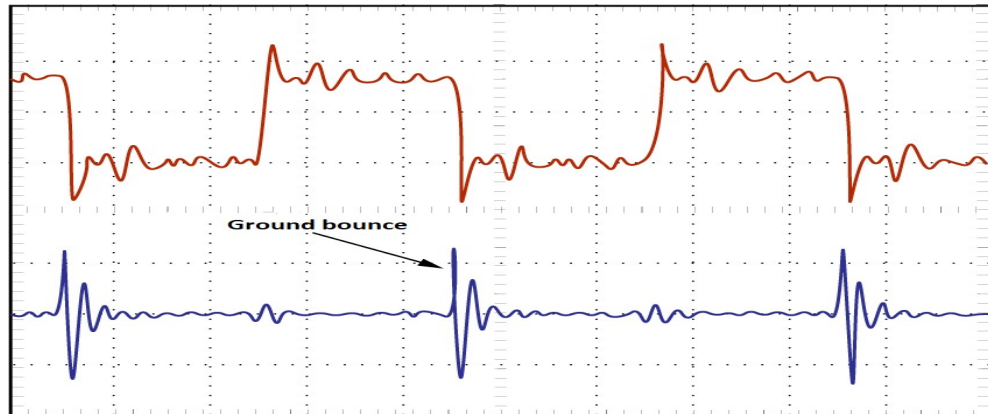
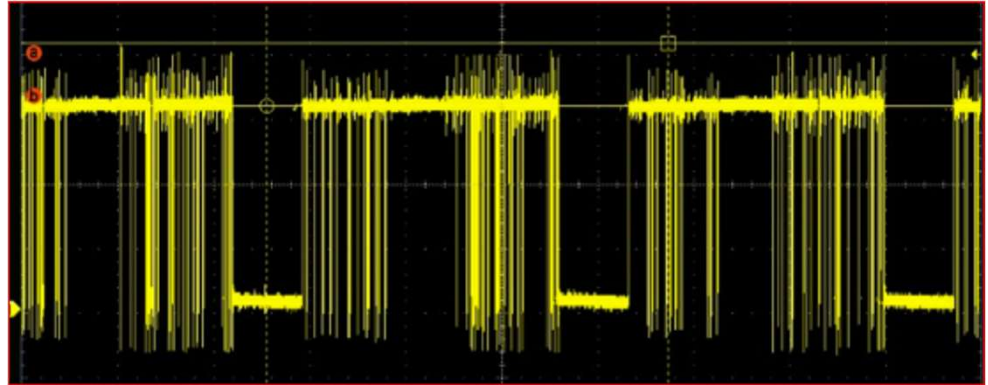
Voltage fluctuations on power rails caused by high-speed switching, insufficient decoupling, or poor PCB layout.



MINIMIZING GROUND BOUNCE

Supply and ground bounce refer to the variations in voltage levels within the power and ground rails of an integrated circuit (IC) die as they relate to their respective positions on the PCB planes. These fluctuations can introduce noise into the system, which may impact logic inputs and outputs, ultimately affecting overall performance. The key factor that drives this issue is the signal edge rate, which can lead to electromagnetic interference (EMI).

With the rapid advancements in CMOS technology and the continued reduction in die sizes, modern ICs showcase much faster switching transitions compared to earlier models. This acceleration makes the effects of intrinsic electrical characteristics, such as inductance in lead frame materials, more significant, resulting in notable supply and ground bounce.



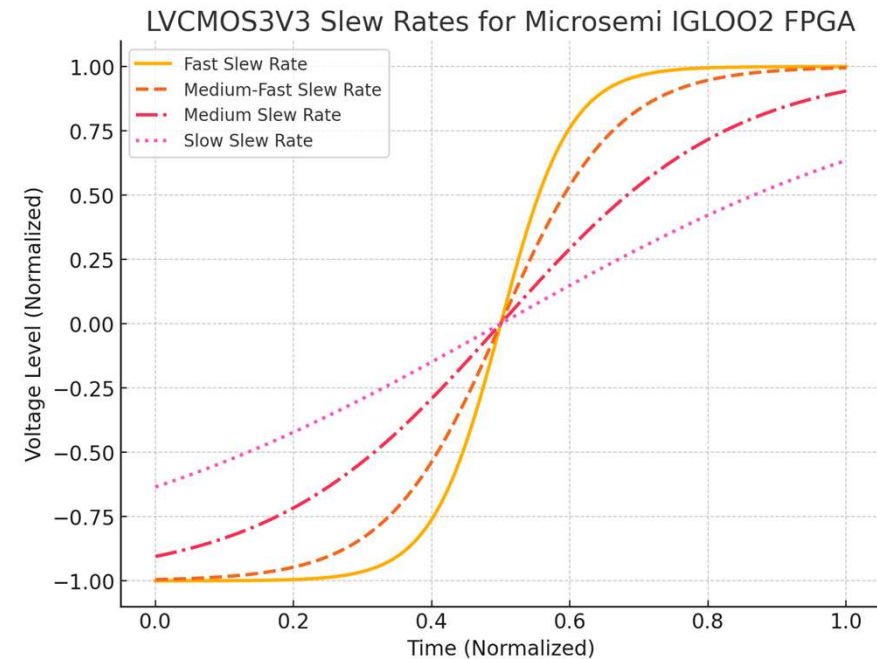
MINIMIZING GROUND BOUNCE USING SLEW RATE CONTROL



To effectively counter these challenges, it is crucial to implement strategic design approaches, especially in high-speed embedded and digital systems. In FPGA designs, for instance, reducing the simultaneous switching of high-speed I/Os can help manage ground bounce; this can be achieved by spreading transitions across various banks.

Additionally, utilizing **slower slew rate** settings can limit transient currents, and avoiding excessive drive strength is advisable unless absolutely necessary.

Maintaining a low-inductance PCB layout is vital, which includes using solid ground planes, minimizing trace lengths, and employing via-in-pad techniques to decrease parasitic inductance. Also, incorporating stitching ground vias near switching I/Os can ensure a consistent return path. A well-designed power and ground plane is essential for providing a stable reference point, which mitigates unwanted voltage fluctuations that could jeopardize timing margins, signal integrity, and the overall reliability of the system.



MINIMIZING GROUND BOUNCE BEST PRACTICES TIPS

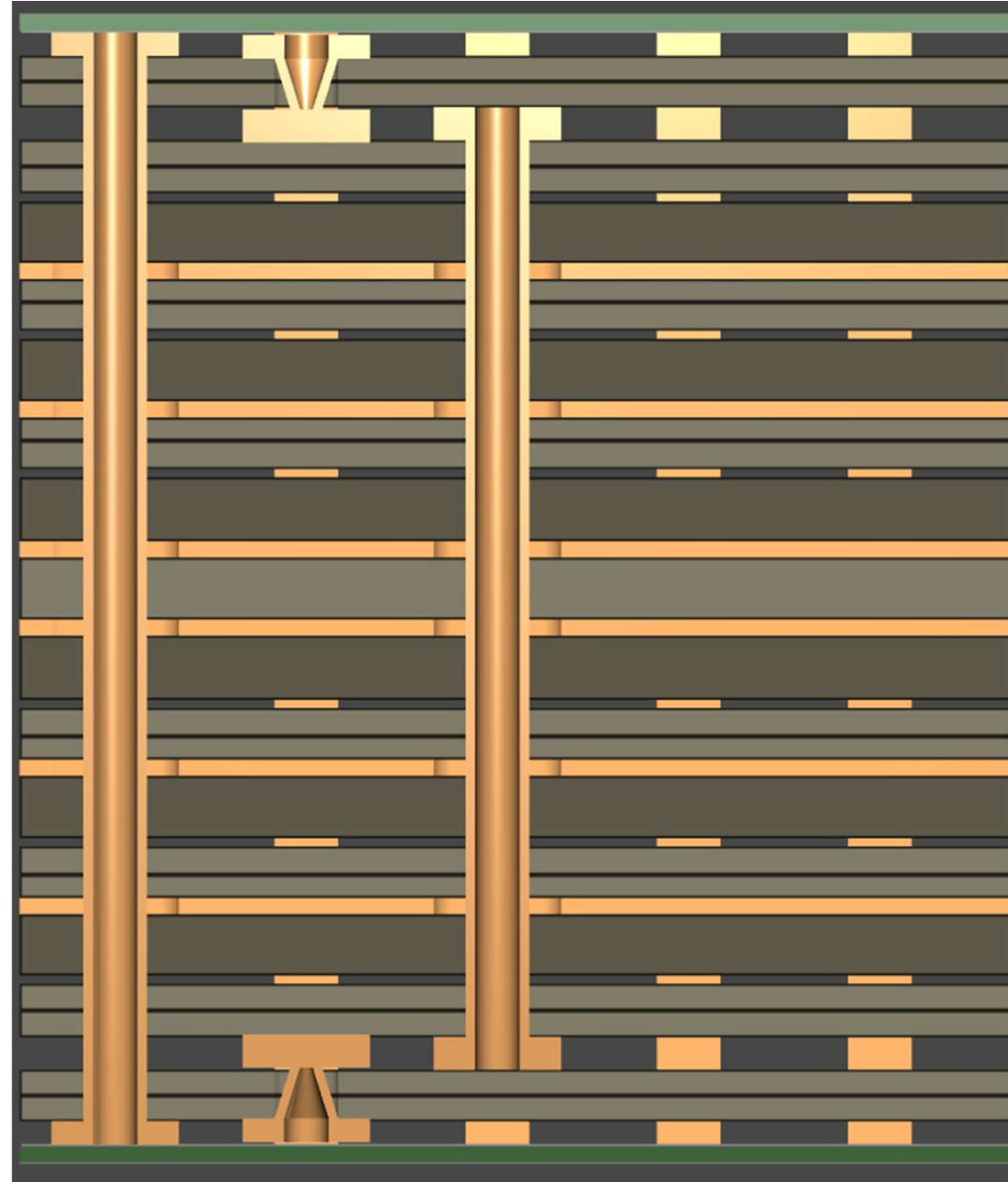


- **Avoid simultaneous switching** of too many I/Os in the same bank.
 - **Distribute switching signals** across different banks to prevent localized current spikes.
 - **Use slow slew rate** settings where possible, especially for non-high-speed signals.
 - **Increase drive strength** only when necessary to avoid excessive current transients.
 - **Use solid ground planes** directly beneath FPGA banks to reduce inductance.
 - **Minimize lead inductance** by using short, wide traces and direct via connections.
 - **Use via-in-pad** techniques for low inductance paths from the FPGA to power planes.
 - **Low-impedance return paths** for high-speed signals.
 - **Power/Ground via stitching** near fast-switching I/Os to ensure a solid return path.
-



OPTIMIZING PCB STACK UP FOR POWER INTEGRITY:

Power integrity is a critical aspect of high-performance PCB design, especially when working with FPGAs and high-speed interfaces. A well-optimized PCB stack up ensures stable power delivery, minimizes noise, and provides solid return paths for signals, reducing electromagnetic interference (EMI) and signal integrity issues. Proper layer arrangement, strategic use of ground and power planes, and careful via placement help maintain low impedance and prevent voltage fluctuations. By optimizing the stack up, designers can enhance power distribution, reduce hotspots, and improve overall system reliability. This presentation explores key techniques to achieve superior power integrity through effective PCB stack up design.



OPTIMIZING PCB STACK UP FOR POWER INTEGRITY:

Key Objectives of Power Integrity Optimization

Minimize power distribution network (PDN) impedance to ensure stable voltage delivery.

Reduce parasitic inductance in power delivery paths.

Improve decoupling efficiency to suppress noise and transients.

Ensure thermal reliability in high-current regions.

Ensuring a solid return path for high-speed signals

- Place continuous ground planes adjacent to high-speed signal layers to provide a low-inductance return path.
- Avoid gaps or splits in ground planes that could force return currents to take longer, more resistive paths.
- Use stitching vias near layer transitions to maintain a consistent return path when signals change layers.

•Using multiple ground connections to minimize impedance mismatches

- Distribute ground vias strategically to reduce loop inductance and improve signal integrity.
 - Maintain a low-impedance power delivery network (PDN) by placing capacitors close to power pins and stitching ground/power planes effectively.
 - Utilize multiple solid ground planes instead of relying on isolated ground islands to ensure a uniform reference potential.
-



OPTIMIZING PCB STACK UP FOR POWER INTEGRITY:

Choosing the Right Stack up Configuration

Your PCB stackup should be designed to provide low-impedance power delivery paths and ensure solid return paths for signals



When possible, try to...

Sandwich power layers between two ground planes to reduce impedance.

Place high-speed signals adjacent to solid ground planes to ensure return path continuity.

Keep power planes close to ground planes to maximize planar capacitance.

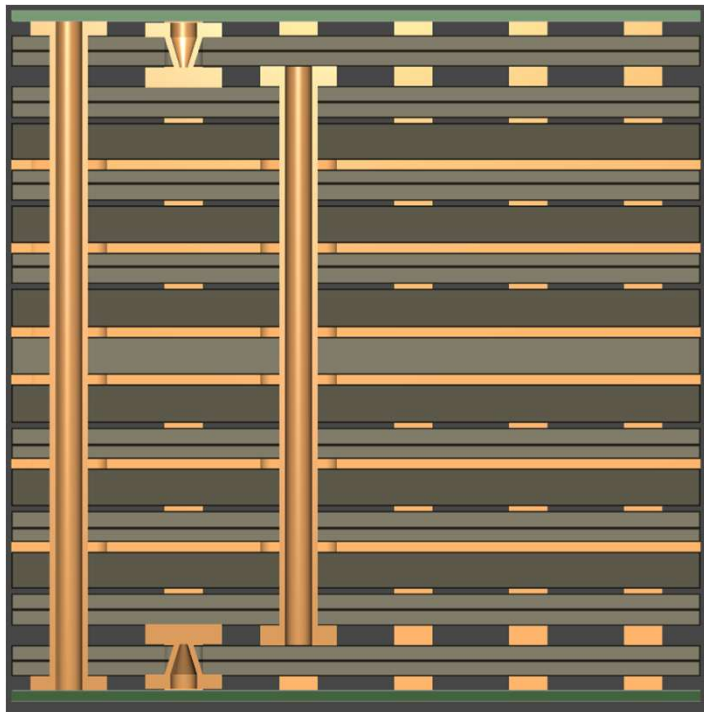
Typical Optimized 12+ Layer Stackup for Power Integrity

Layer	Function
L1	Signal (High-speed)
L2	Ground (Solid Reference)
L3	Signal (High-speed, Controlled Impedance)
L4	Power (VCC Plane)
L5	Ground (Reference for L6)
L6	Mixed-Signal / Low-Speed Signals
L7	Ground (Reference for L8)
L8	Power (Secondary VCC)
L9	Signal (High-Speed)
L10	Ground (Reference for L9)
L11	Signal (High-Speed)
L12	Ground (Solid Reference)

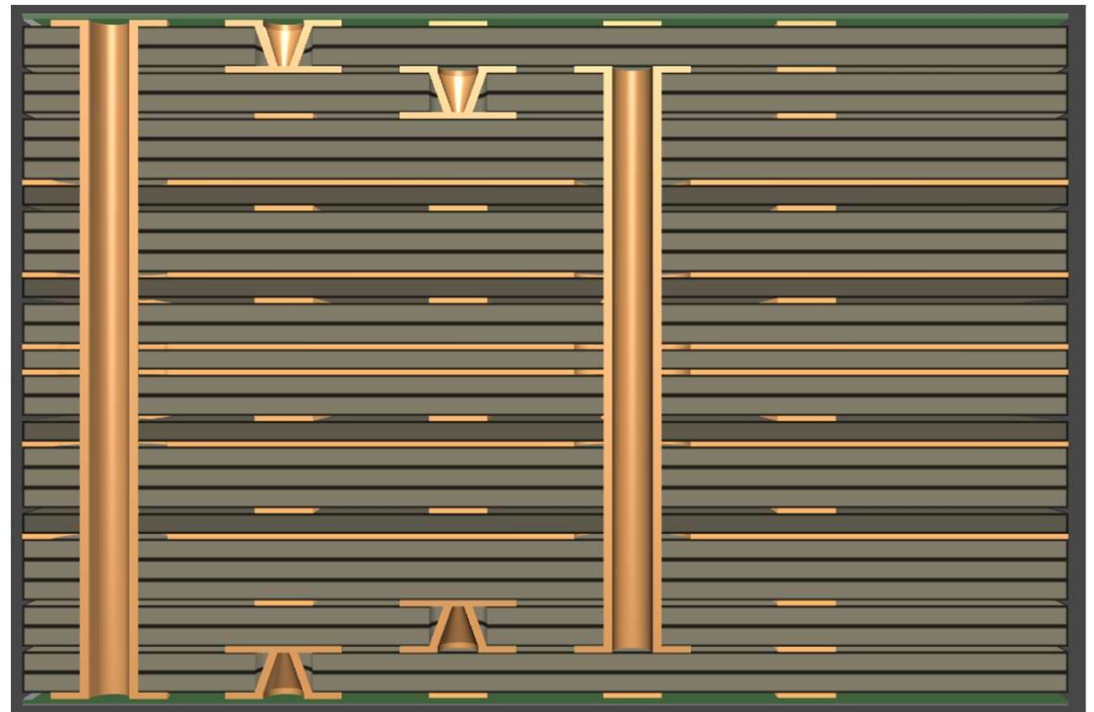


EXAMPLE LAYER STACKS USED AND TESTED

16 layers 1.6mm PCB thickness



16 layers 1.6mm PCB thickness



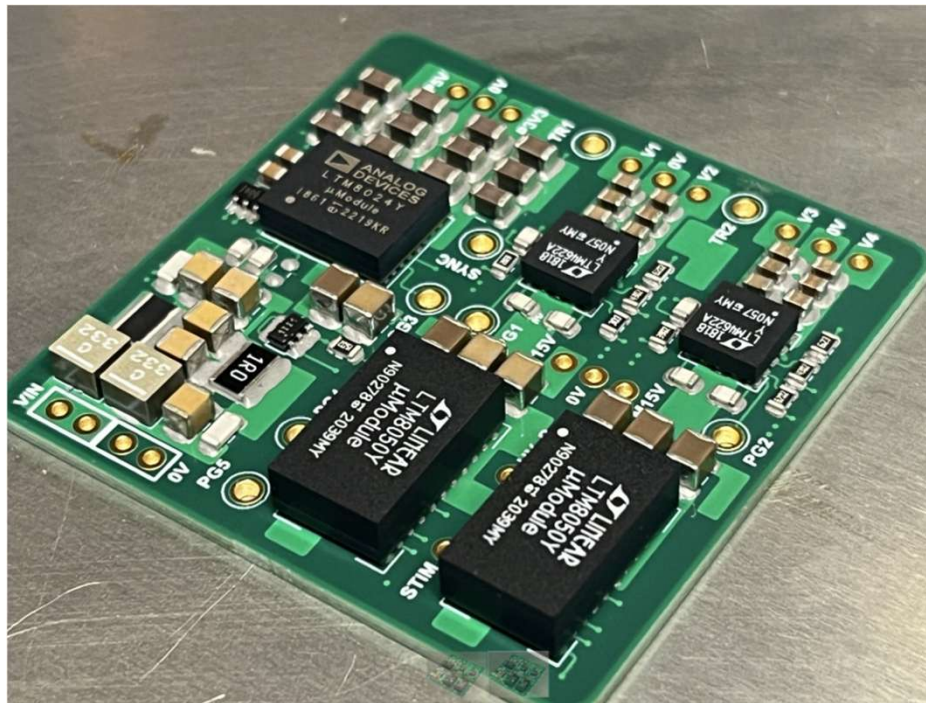
A FEW
EXAMPLES
BUILT IN MY
OWN LAB



EXAMPLE OF COMPONENT PLACEMENT OPTIMISED FOR PDN



MODULAR VRM FOR DEMO DESIGNS



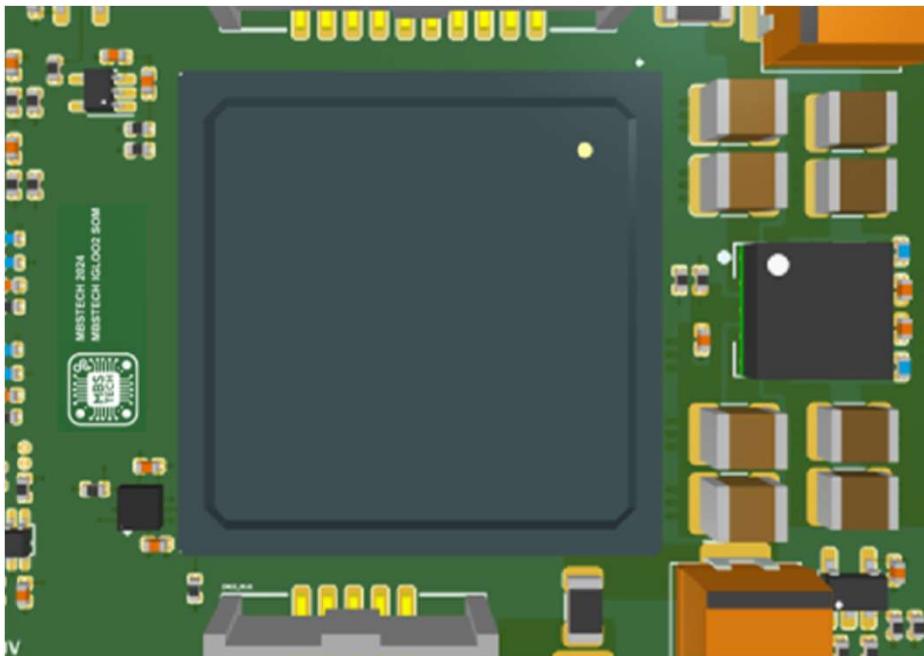
MODULAR VRM FOR DEMO DESIGNS



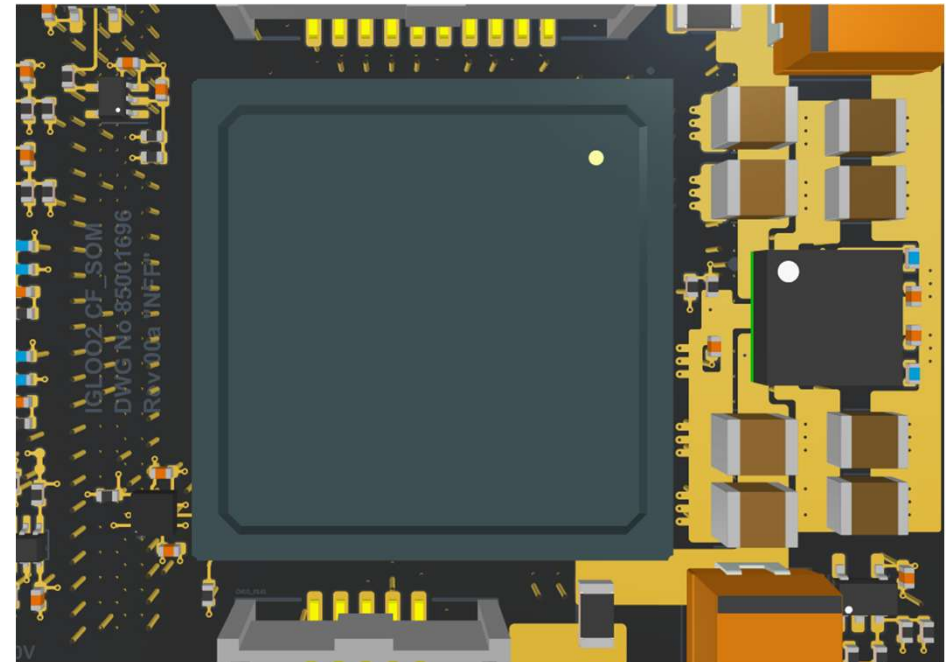
EXAMPLE OF COMPONENT PLACEMENT OPTIMISED FOR PDN



3D VIEW TOP OF BOARD



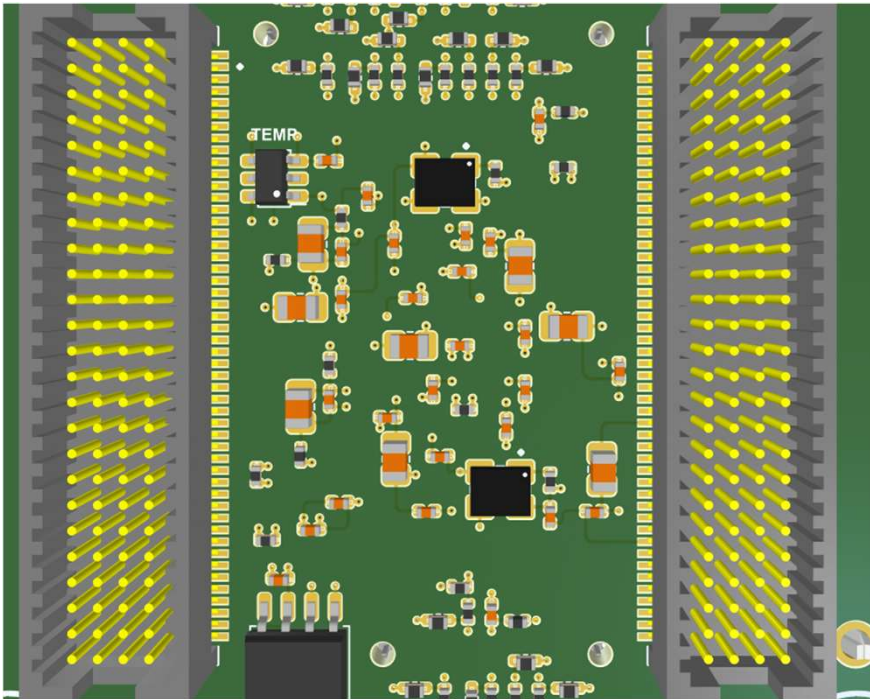
COPPER VIEW TOP OF BOARD



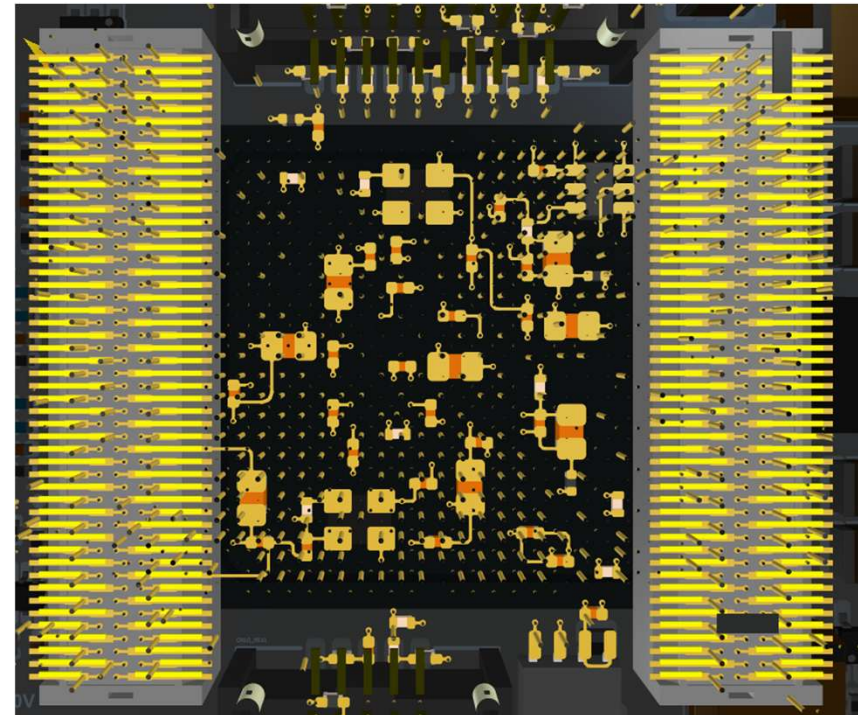
EXAMPLE OF COMPONENT PLACEMENT OPTIMISED FOR PDN



3D VIEW BOTTOM OF BOARD



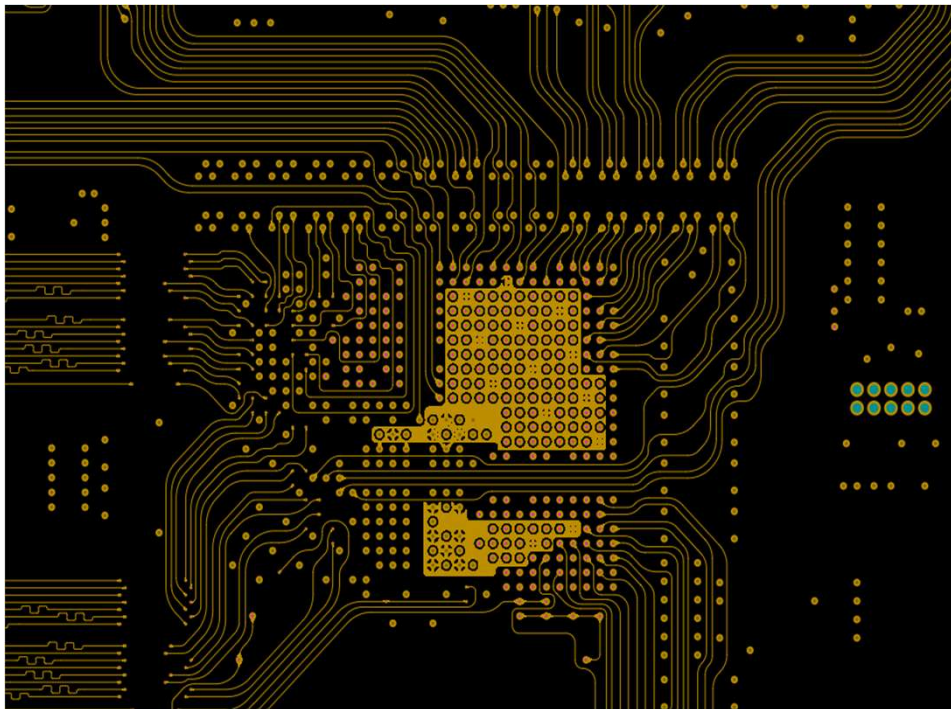
COPPER VIEW BOTTOM OF BOARD SHOWING DECOUPLING



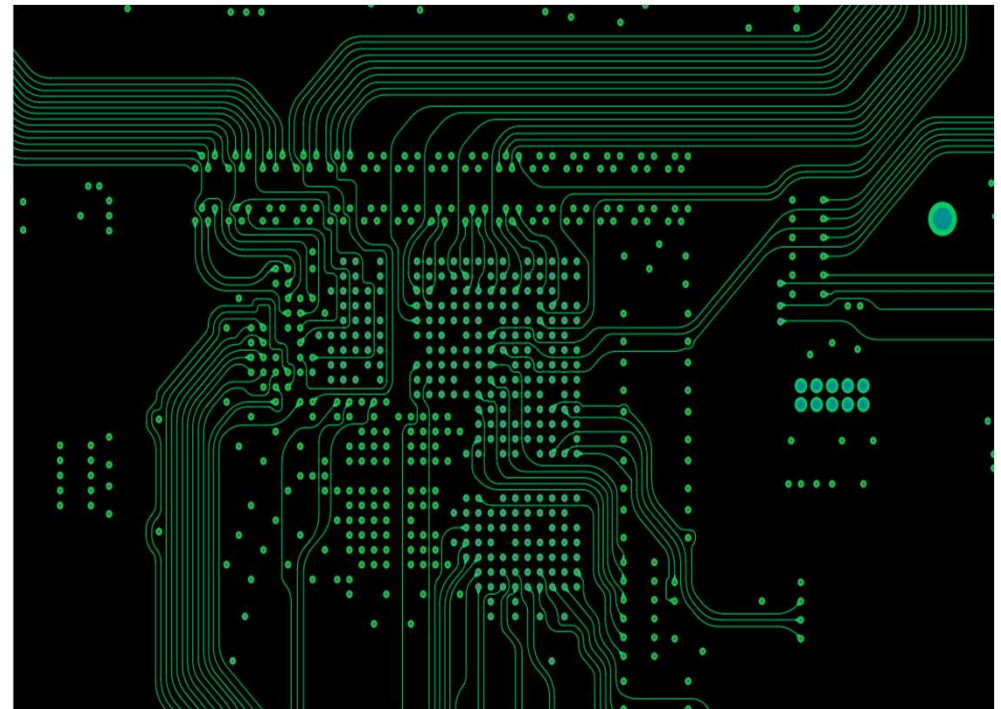
EXAMPLE OF POINT-TO-POINT MONOTONIC ROUTING CLASSIC ROUTING VIEW



OPTIMISES IMPEDANCE CONTROL



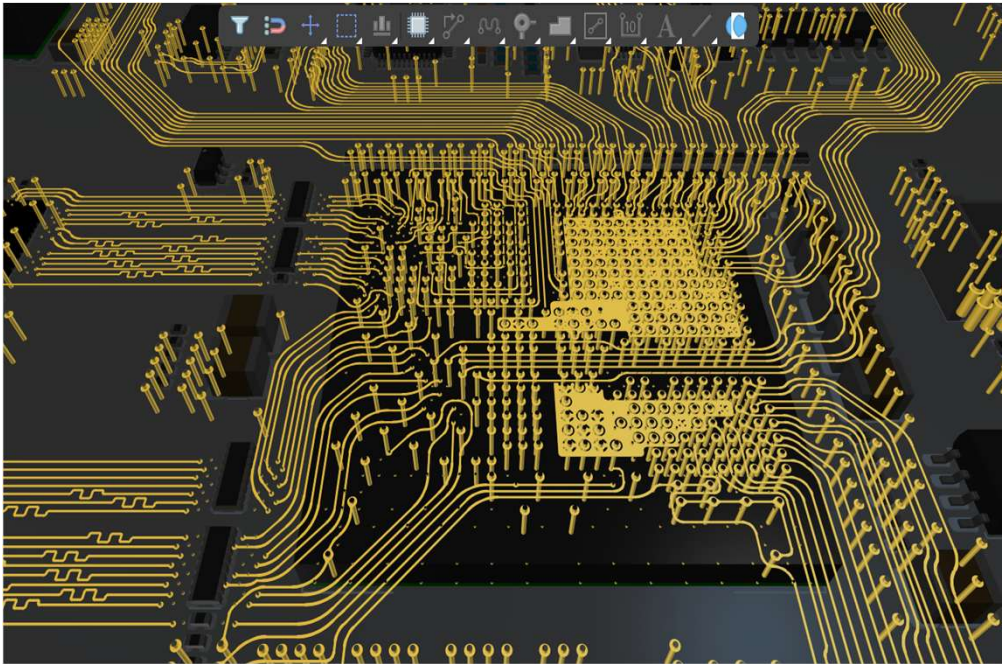
MINIMISES PARASITICS



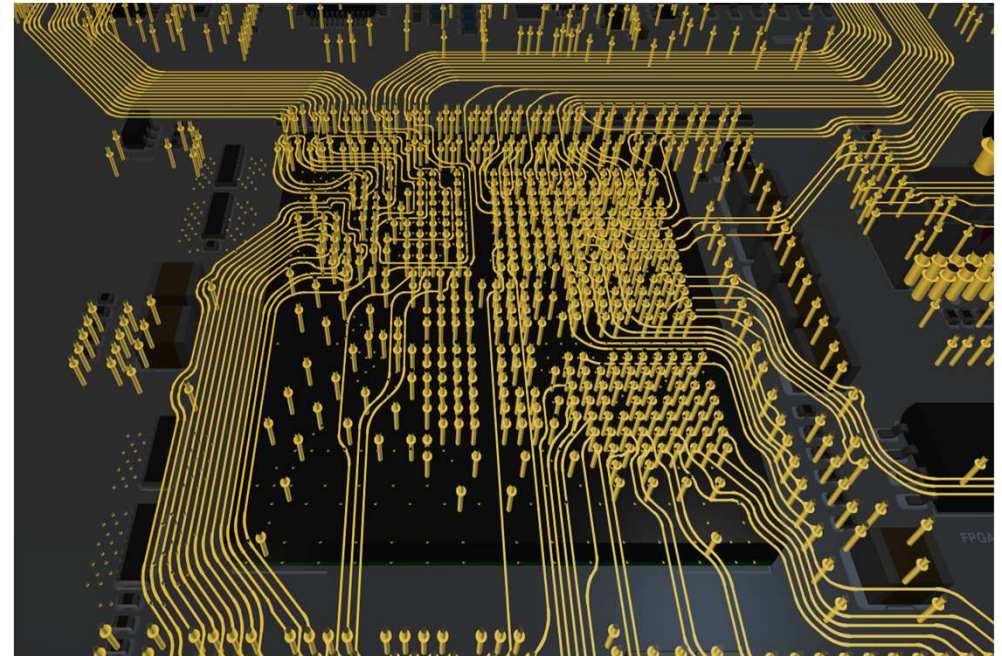
EXAMPLE OF POINT-TO-POINT MONOTONIC ROUTING COPPER LAYER VIEW



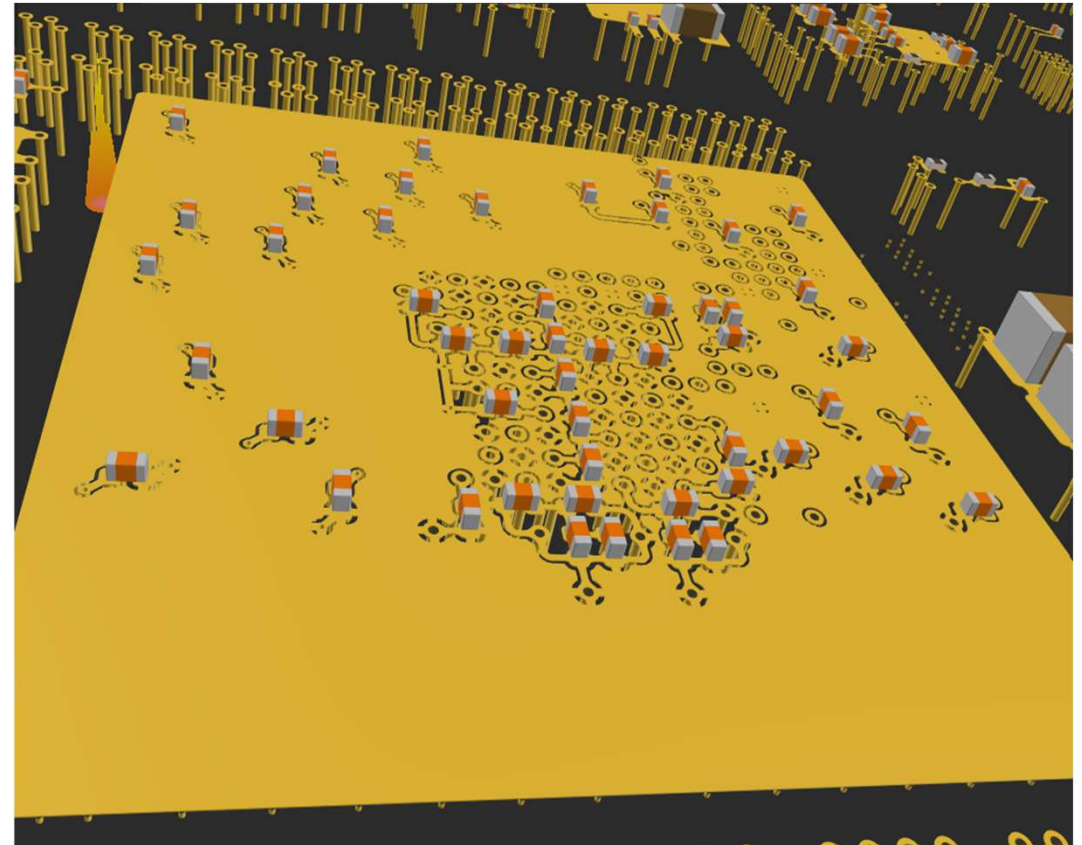
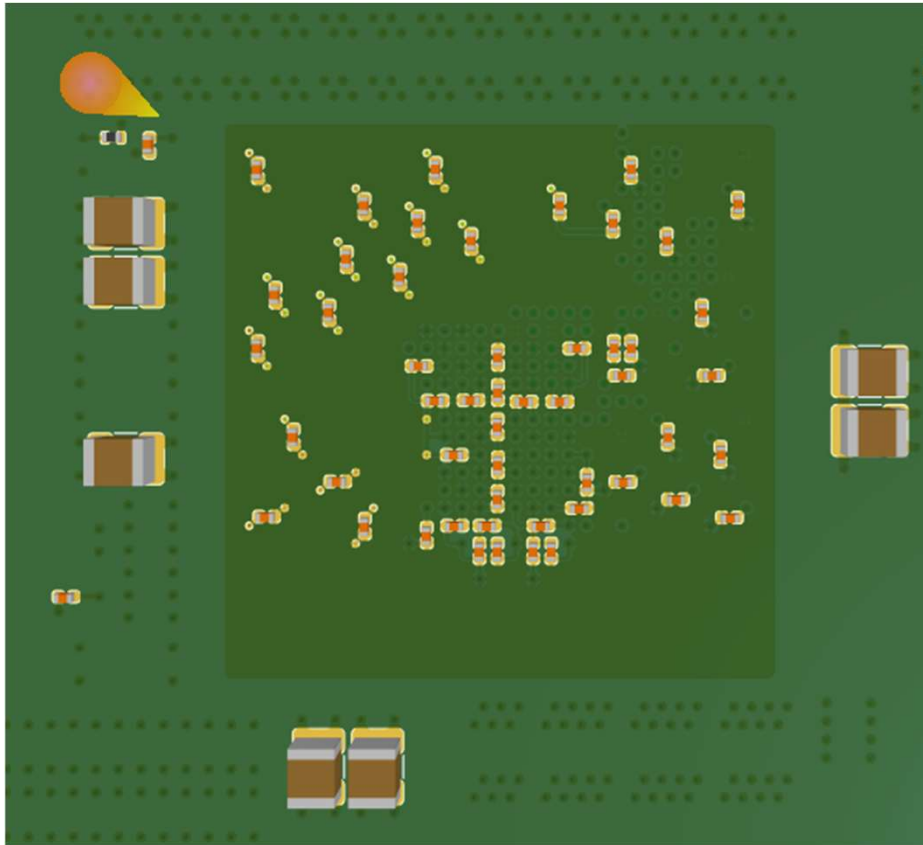
OPTIMISES IMPEDANCE CONTROL



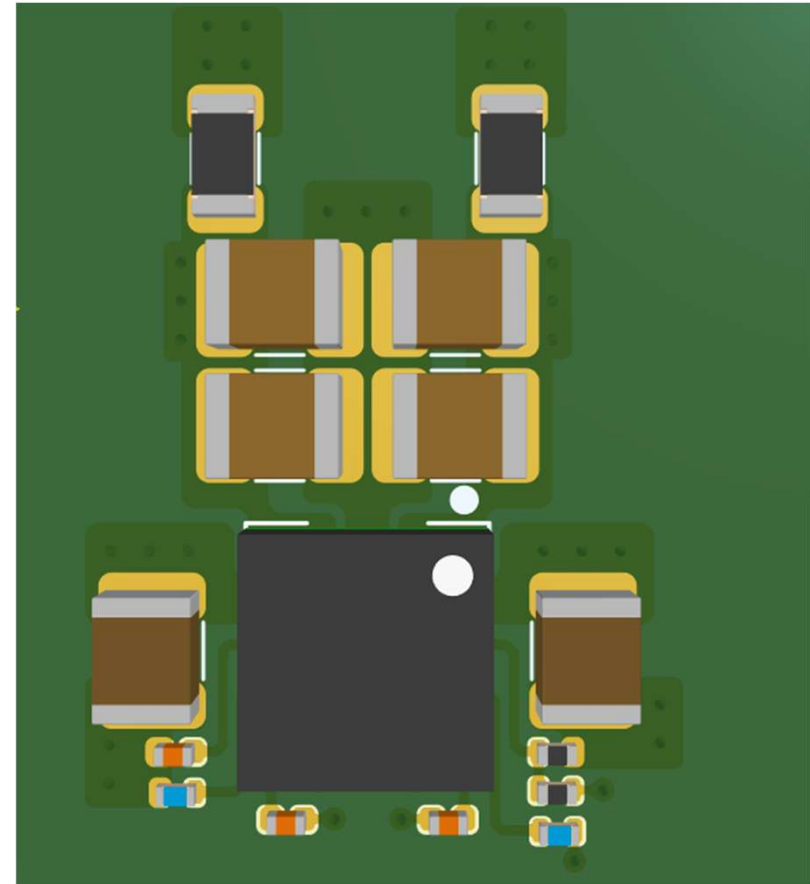
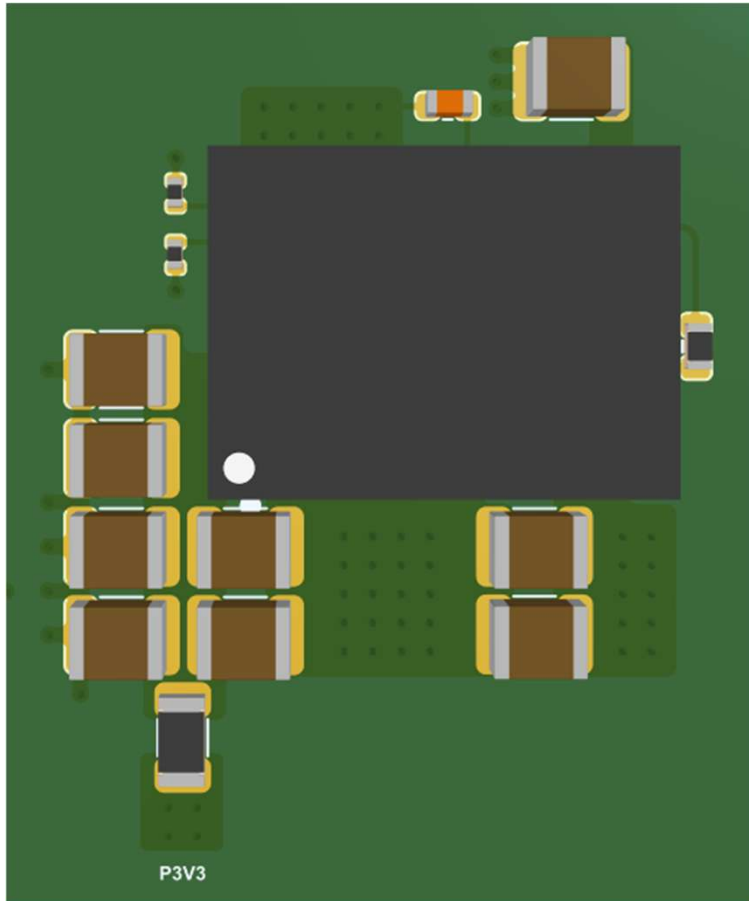
MINIMISES PARASITICS



OPTIMISED PLACEMENT OF CORE AND I/O FPGA DECOUPLING CAPACITORS



EXAMPLES OF VRM'S COMPONENT PLACEMENT



EXAMPLES OF VRM'S COPPER VIEW PLACEMENT AND VIA SEEDING

