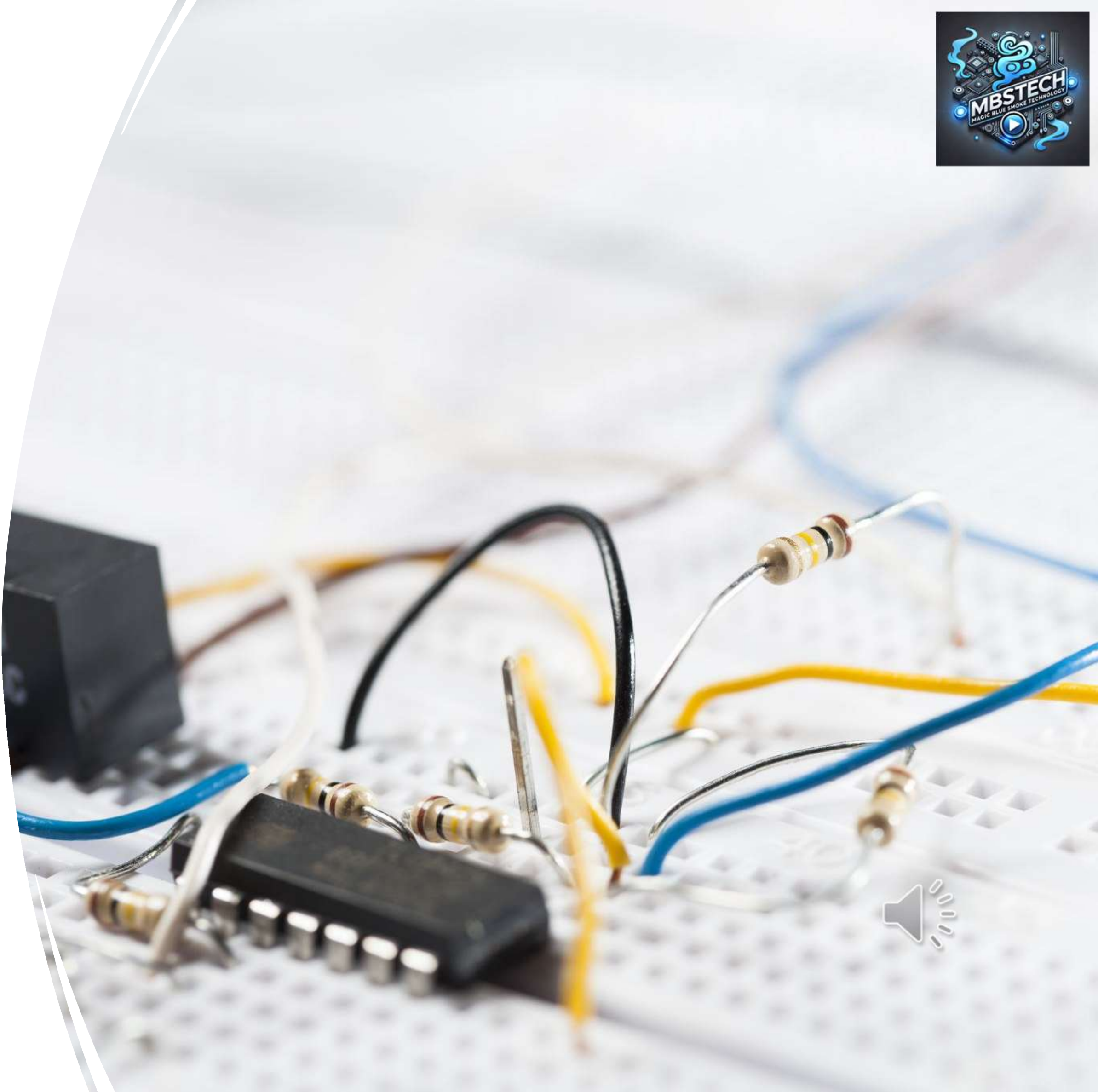
Electronics Toolbox Advice

Understanding capacitors and their usage from the perspective of an FPGA.

- Power Point Created By
- Andy Carpenter 2025



Decoupling and Bypass WHAT’s Different ?

Are they different ?

- Decoupling capacitors and bypass capacitors are often confused due to their interconnected uses, yet they serve distinct purposes.
- **Decoupling capacitors** ensure voltage stability by supplying transient current.
- **Bypass capacitors** eliminate noise by directing it to ground.
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  It is important to note that in real-world scenarios, a single capacitor frequently fulfils both roles, which contributes to the interchangeable use of the terms.
- Although both types of capacitors contribute to noise reduction and voltage stability, **decoupling capacitors** primarily focus on maintaining power integrity and preventing cross-interference, whereas **bypass capacitors** specifically filter out high-frequency noise by diverting it to ground. Nonetheless, many capacitors can perform both functions concurrently.
- In discussions about design, "decoupling" tends to stress transient response and stability, while "bypass" concentrates on noise reduction.

Decoupling Capacitors

- **Purpose:** Decoupling capacitors serve to "decouple" various sections of a circuit, acting as a local energy source that can deliver transient currents.
- **Function:** Their primary function is to stabilize the power supply voltage by accommodating swift changes in current needs, thereby averting voltage drops or surges.
- **Placement:** These capacitors are generally positioned close to the power pins of integrated circuits (ICs), particularly in applications involving high-speed digital and mixed-signal systems.
- **Frequency Response:** A variety of capacitance values are employed in parallel to address a wide frequency spectrum—smaller capacitors (like 100nF and 1nF) manage high-frequency noise, while larger capacitors (such as 10μF and 100μF) help stabilize lower-frequency variations.

Bypass Capacitors

- **Purpose:** Bypass capacitors are designed to "bypass" alternating current (AC) noise or high-frequency signals from the power supply to the ground, effectively preventing interference with delicate components.
- **Function:** They act as a short circuit for high-frequency noise, redirecting it to the ground and ensuring that the circuit receives uninterrupted, clean power.
- **Placement:** These capacitors are usually situated close to the power pins of integrated circuits (ICs) and are especially beneficial in applications aimed at noise reduction.
- **Frequency Response:** Their main function is to mitigate high-frequency noise, and they typically consist of small capacitors (such as 100nF or 1nF) with low equivalent series resistance (ESR) to preserve high-speed signal integrity.

Key Differences Table

Feature	**Decoupling Capacitor**	**Bypass Capacitor**
Purpose	Isolates circuit sections to prevent noise interference	Provides a low-impedance path for high-frequency noise
Effect	Smooths voltage variations	Eliminates high-frequency noise
Placement	Close to IC power pins	Across power supply rails
Functionality	Stabilises voltage supply	Filters out AC noise

Decoupling for FPGA's

- A well-designed FPGA power system typically uses a combination of capacitors with different values to cover a wide frequency range of noise suppression:

Capacitor Value	Purpose	Placement
0.1µF - 0.47µF	High-frequency noise filtering (100 MHz – 1 GHz)	Close to each power pin
1µF - 10µF	Mid-frequency transient suppression (1 MHz – 100 MHz)	Spread evenly across power pins
10µF - 100µF	Bulk capacitors for low-frequency noise and large current demands (below 1 MHz)	Near power supply input

What are the Reasons for Using Various Decoupling Capacitor Values?

- The choice of decoupling capacitors is affected by variations in **switching frequency**, **current requirements**, and **voltage stability needs**.

Feature	**Core Voltage (VCC_CORE)**	**I/O Voltage (VCC_IO)**
Voltage Level	Lower (0.8V – 1.2V)	Higher (1.8V – 3.3V)
Current Demand	Higher (due to dense logic switching)	Lower (depends on active I/Os)
Switching Speed	Very High Frequency (hundreds of MHz to GHz)	Moderate (tens to hundreds of MHz)
Noise Sensitivity	Very Sensitive	Less Sensitive
Voltage Tolerance	Tight regulation needed	More tolerant to fluctuations
Capacitor Type	Small-value capacitors (0.1µF, 1µF) to handle high-frequency transients	Larger-value capacitors (1µF, 10µF, 22µF) to filter lower-frequency transients

Core Voltage vs I/O Voltage in an FPGA

Core Voltage (VCC_CORE)

The core voltage is essential for powering the FPGA's **logic fabric, internal clocks, DSP blocks, and memory**.

- Typically, it operates at a **low voltage** (e.g., **0.8V – 1.2V**) while drawing **high current**, as modern FPGAs consist of thousands or millions of logic elements that switch rapidly.
- The core logic **operates at high frequencies**, leading to the generation of considerable high-frequency transients.
- **Tight voltage regulation is necessary** because minor voltage fluctuations can result in instability within the logic operations.

I/O Voltage (VCC_IO)

The I/O voltage supplies power to the **input/output buffers of the FPGA**, which manage external signals.

- Typically, this voltage is **higher** (for instance, **1.8V – 3.3V**) and relatively characterized by **lower current**, influenced by the number of I/O pins that are toggling.

- The **switching speeds tend to be slower** compared to core logic, depending on the specific interface standard (such as LVTTL, LVDS, etc.).

- I/O banks accommodate **larger voltage variations** but have less stringent requirements for transient response than the core.

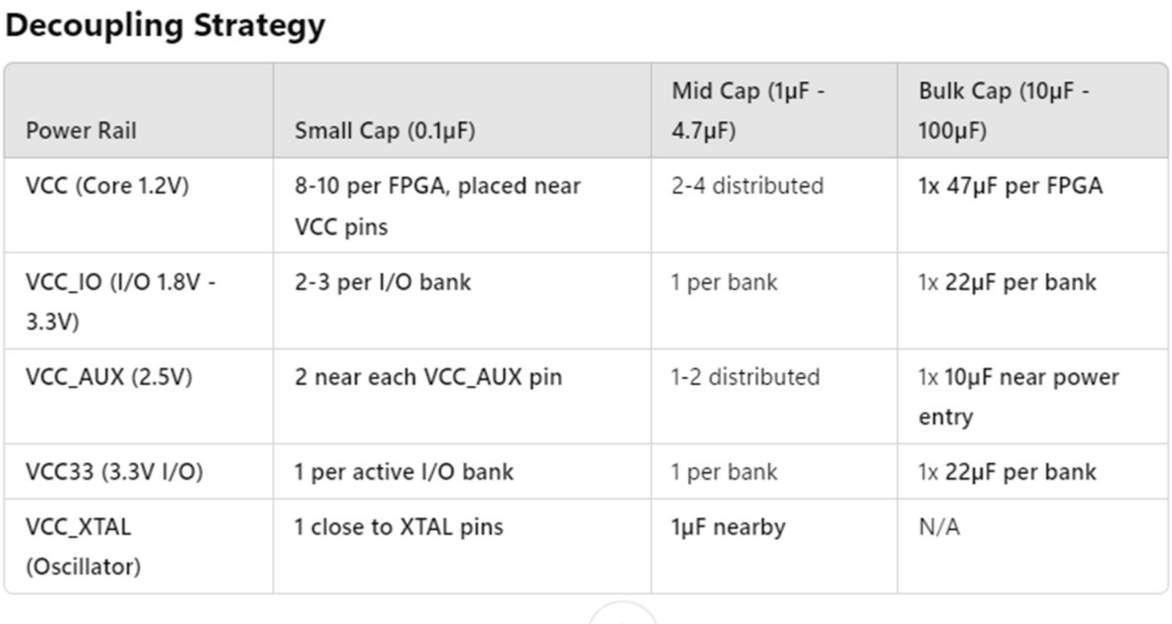
Key Considerations

- **Use multiple capacitors in parallel**: Implementing a range of capacitor values helps achieve effective performance across a broad frequency range.
- **Choose low-ESR ceramic capacitors**: It is advisable to use Multi-Layer Ceramic Capacitors (MLCC) with X7R dielectrics avoid the use of X5R for aerospace applications.
- **Place capacitors close to the FPGA power pins**: Doing so reduces power rail impedance and improves transient response.
- **Include several ground vias**: This practice decreases inductance and enhances the capacitors' effectiveness.

Example Solution for Microsemi Parts IGLOO2

For the **Microsemi IGLOO2 FPGA**, the recommended **decoupling capacitor strategy** follows standard best practices for FPGA power integrity while considering its **low-power Flash-based architecture**. Below is an **optimized decoupling scheme** based on IGLOO2's power rails.

- Since **IGLOO2 FPGAs have a lower power draw** than SRAM-based FPGAs (e.g., Xilinx or Intel/Altera), their **decoupling requirements are slightly less aggressive**. However, a solid decoupling plan is still needed for power integrity.



Decoupling Strategy

Power Rail	Small Cap (0.1µF)	Mid Cap (1µF - 4.7µF)	Bulk Cap (10µF - 100µF)
VCC (Core 1.2V)	8-10 per FPGA, placed near VCC pins	2-4 distributed	1x 47µF per FPGA
VCC_IO (I/O 1.8V - 3.3V)	2-3 per I/O bank	1 per bank	1x 22µF per bank
VCC_AUX (2.5V)	2 near each VCC_AUX pin	1-2 distributed	1x 10µF near power entry
VCC33 (3.3V I/O)	1 per active I/O bank	1 per bank	1x 22µF per bank
VCC_XTAL (Oscillator)	1 close to XTAL pins	1µF nearby	N/A

PCB Layout Recommendations for Decoupling IGLOO2 FPGA

To ensure **optimal power integrity and signal integrity,** follow these best practices for **placing and routing decoupling capacitors** in an **IGLOO2 FPGA PCB design**.

•General Placement Strategy

•**Place capacitors as close as possible to power pins**:

•**0.1µF (100nF) caps** should be **within 2 – 4 mm** of FPGA power pins.

•**1µF - 4.7µF caps** should be **within 5 – 8 mm** of FPGA power rails.

•**Bulk capacitors (10µF - 100µF)** should be **near power entry points or regulators**.

•**Distribute capacitors around the FPGA**:
•Do not cluster capacitors on one side—spread them evenly.

•**Use the shortest possible traces** to connect capacitors to power and ground where possible!!!

Additional PCB Design Best Practices Part 1

- **Conduct power integrity simulations** to confirm the placement of capacitors.
- **Prevent multiple ground islands** by employing a **single, uninterrupted ground plane**.
- **Reduce the loop area** between power and ground connections.
- **Select Low-ESR MLCC capacitors** X7R for optimal performance.
- Strive to minimize via inductance.
- **Employ thick traces or wide polygons** for power connections.
- **Always maintain a solid ground plane beneath the FPGA** to ensure low impedance return paths.
- **Implement split power planes for different voltage domains** (VCC, VCC_IO, PLL).
- **Core Voltage (VCC 1.2V)**
  - **Use a compact configuration of 0.1μF capacitors** around the FPGA.
  - **Ensure that vias connect directly to a solid ground plane** (to prevent lengthy traces).

Additional PCB Design Best Practices Part 2

- **It is crucial to remember** that **low-inductance power delivery** is vital for **rapid logic switching**.
- **Consider the sensitivity to noise in clock circuits**, which requires a **low-noise power supply**.
- Ferrite beads (600Ω @ 100MHz) can effectively mitigate power noise; however, caution is advised as they might cause voltage droop by limiting the high-frequency current necessary for modern integrated circuits. When using ferrite beads, ensure that local decoupling is implemented at the specific load point of interest.
- **Refrain from crossing power domains close to SERDES lanes**.
- **Conduct IR drop analysis** to verify the reliability of power distribution.
- **Utilise decoupling capacitor optimization tools** (e.g., ANSYS, HyperLynx PI).
- Measure **power rail noise** with a **high-bandwidth oscilloscope** (≥1GHz).
- Evaluate **transient response** by adjusting FPGA loads.

Why Are Vias and Power Planes Important in FPGAs?

Incorrect via clearances beneath a **Ball Grid Array (BGA) FPGA** can lead to **power plane pinching**, which adversely affects both **power integrity (PI)** and **signal integrity (SI)**. Below is a thorough explanation of the issue and its implications.

What is Power Plane Pinching?

Power plane pinching refers to the phenomenon where **vias are positioned too closely together under a BGA**, which diminishes the effective **copper area of the power plane**. This situation **constricts current pathways**, resulting in **elevated resistance and inductance**, thereby impairing power delivery to the FPGA.

Causes of Power Plane Pinching

- **Closely spaced via anti-pads (clearances) within power layers**
- **Excessive overlap of ground/power via clearances**
- **Insufficient copper remaining in the power plane due to high via density**
- **Inefficiently sized vias, clearances, and plane connections**

Effects of Power Plane Pinching

Elevated Power Supply Impedance

- Power plane pinching **diminishes the effective copper area**, resulting in **increased DC resistance and AC impedance**.
- A **power plane with higher impedance** fails to deliver **low-noise, stable power** to the FPGA core and I/O circuits.
- This **compromises the efficiency of decoupling capacitors**, causing a **deterioration in transient response**.

Reduced Thermal Dissipation

- Power planes **help distribute heat**. If they are heavily pinched, they **lose thermal conductivity**, increasing FPGA **hot spots**.
- **High temperatures lead to reduced reliability and potential failure** over time.

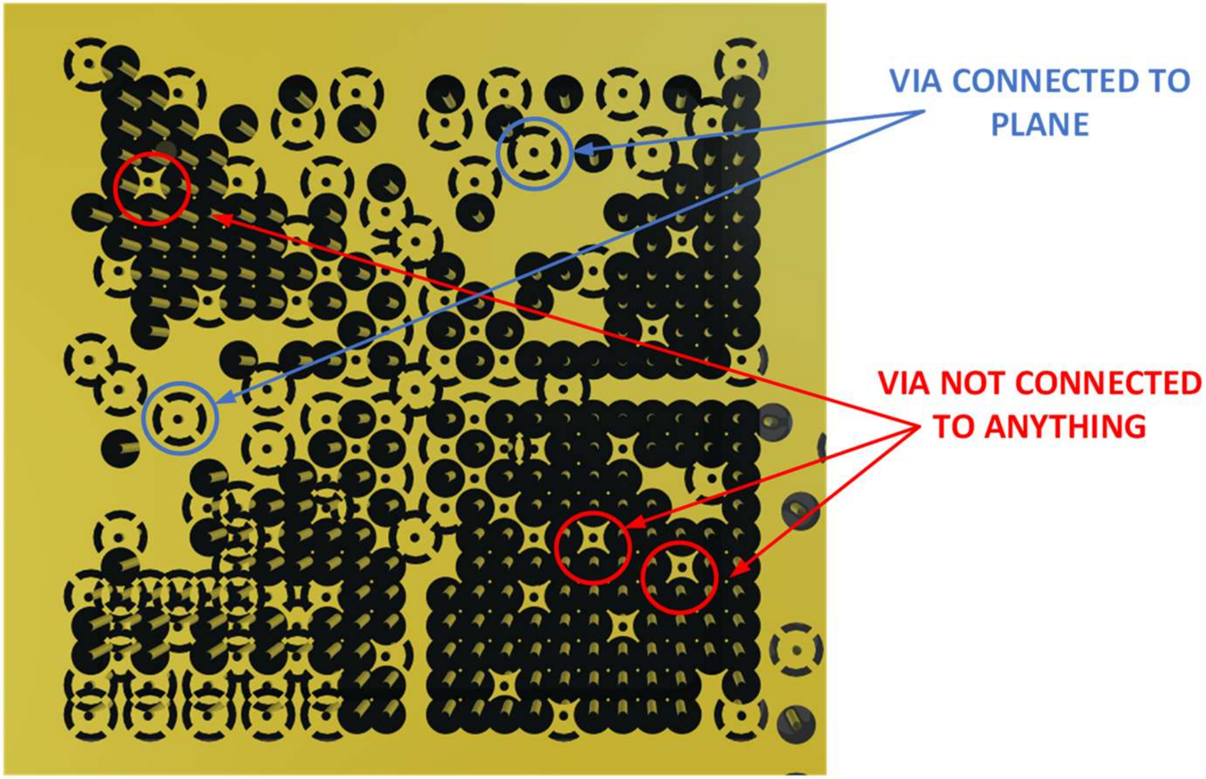
Voltage Drop (IR Drop) Concerns

- Constricted power planes **limit current flow**, resulting in significant **voltage drops** (IR drop).
- Voltage variations may lead to **unstable operation** in FPGA logic and high-speed I/Os.

Elevated Ground Bounce & Noise

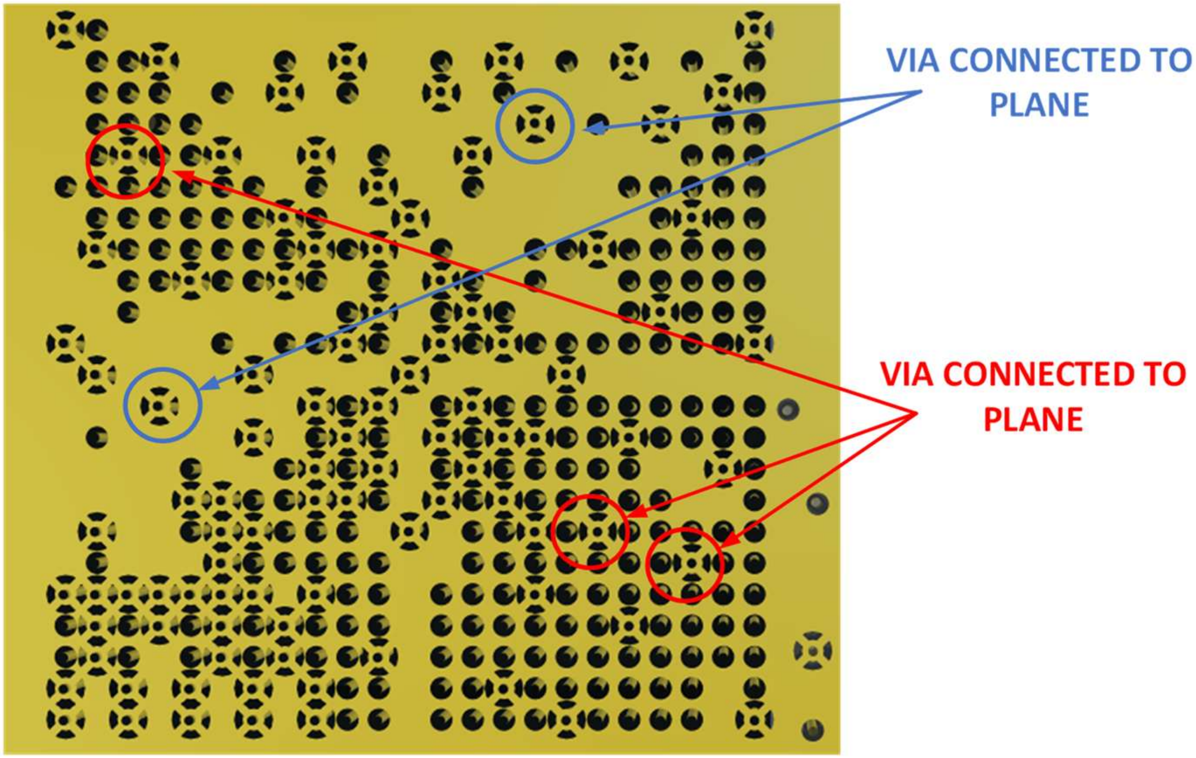
- **Constricted return current paths amplify loop inductance**, contributing to **ground bounce and signal interference**.
- **High-speed circuits (DDR, SERDES, PLLs) are particularly susceptible** to power noise stemming from inadequate plane integrity.

Vias and Power Planes under FPGA’s



A problem arose because the clearance for the via in the power plane was incorrect.

Vias and Power Planes under FPGA’s



VIA CONNECTED TO PLANE

VIA CONNECTED TO PLANE

The problem was addressed by guaranteeing adequate clearance of the power plane for the via.

Best Practices to Avoid Power Plane Pinching

Enhance Performance Through Clearance and Anti-Pads

✅ **Ensure adequate copper is maintained in the power plane** to facilitate proper current flow.
✅ **Apply larger anti-pad clearances only where absolutely necessary** (avoid excessive clearance).
✅ **Opt for staggered via positioning** rather than concentric arrangements to enhance plane connectivity.

Preserve Low Impedance in Power Planes

✅ **Minimise plane cutouts** to **prevent disruption of current paths.**
✅ **Utilize wider power plane traces whenever feasible** to **reduce resistance.**
✅ **Incorporate multiple ground return vias for each power via** to **lower loop inductance.**

Utilise Dedicated Power and Ground Layers

✅ **Allocate an entire PCB layer for power and another for ground** to ensure consistent low-impedance planes.
✅ **Minimise excessive segmentation of planes beneath the FPGA** to preserve **power continuity.**
✅ **Conduct power integrity (PI) simulations (IR drop, impedance analysis)** to pinpoint vulnerabilities.

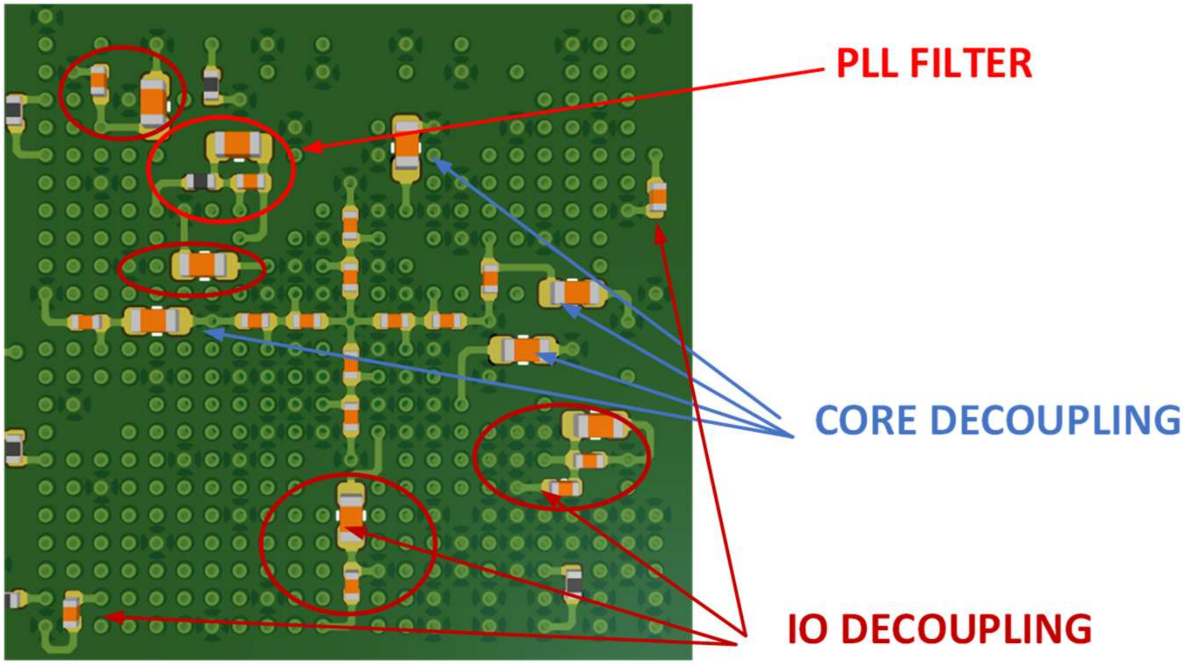
Enhance BGA Escape Routing for Power Integrity

✅ **Implement via-in-pad (VIP) for power vias** to **lessen the clearance effect on planes.**
✅ **Strategically distribute power vias** instead of grouping them in a single location.
✅ **Position decoupling capacitors near power vias** to mitigate localized impedance fluctuations.

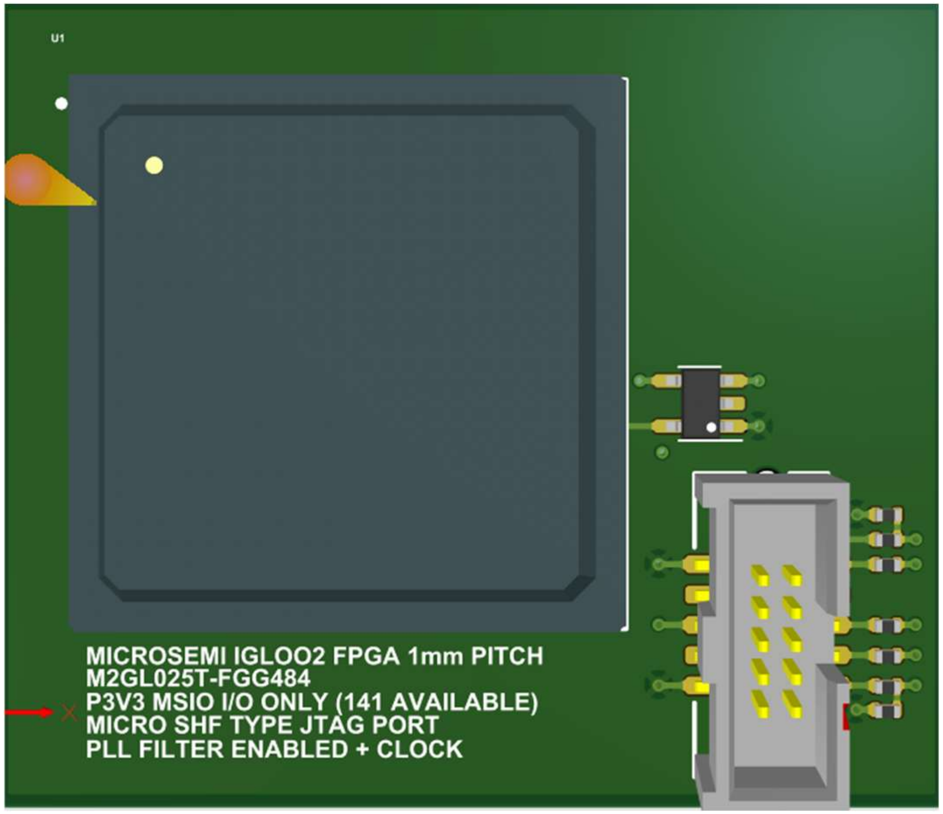
Remember poor power plane integrity means high inductive / impedance PDN resulting in poor performance…

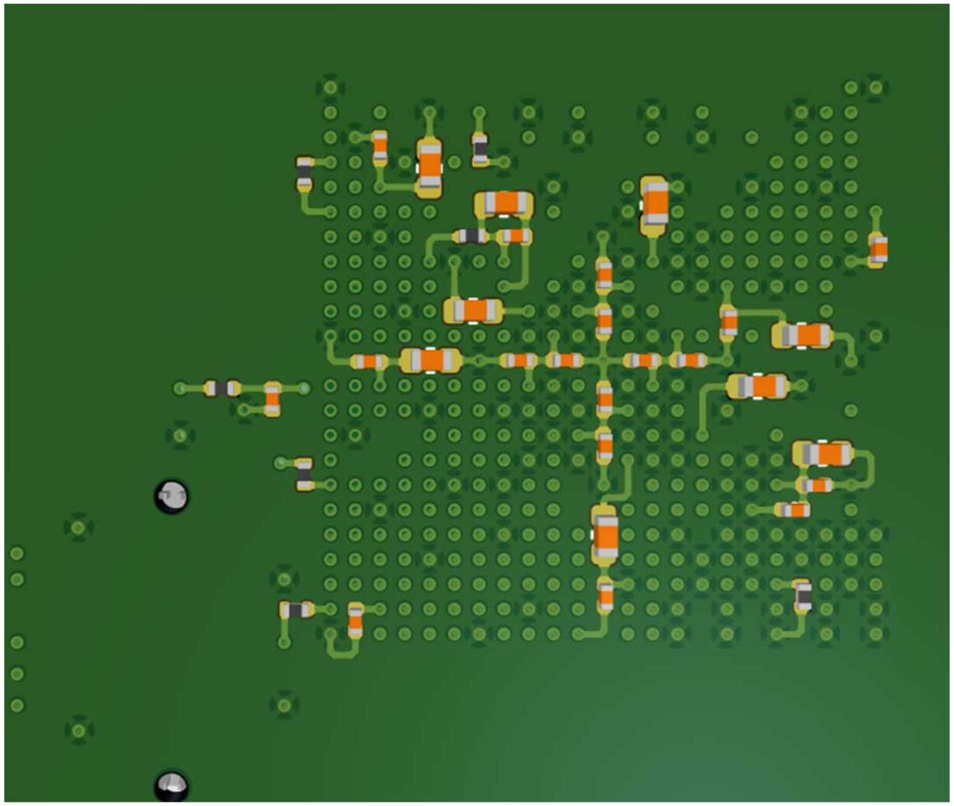
Example of Decoupling Placement under BGA

- In the picture shown the FPGA a M2GL025 has been designed so that
- only the MSIO pins are used @ P3V3 voltage level.
- PLL Filter is provided for.
- Core P1V2 decoupling provided for.
- All configuration resistors for example
  - JTAGSEL
  - DEVRST_N
  - FLASH_GOLDEN
  - JTAG
  - MSIOD VCC KEEPER



FPGA Featuring JTAG Interface and Decoupling





Package Sizes for Decoupling Under a BGA FPGA

The **optimal capacitor package size** for decoupling under a **BGA FPGA** is a balance between **low inductance, space constraints, manufacturability, and thermal stability**. Below is a breakdown of the best choices:

Package Size	Dimensions (mm)	Advantages	Common Usage Under BGA
0201 (0603 metric)	0.6 x 0.3	Ultra-low inductance, best for GHz-range decoupling	Best for **high-density FPGA designs**, close to power pins
0402 (1005 metric)	1.0 x 0.5	Low inductance, still small enough for tight layouts	**Most commonly used** for FPGA core decoupling
0603 (1608 metric)	1.6 x 0.8	Lower ESR, easier to place than 0402	Good for **mid-range decoupling**, placed slightly farther away
0805 (2012 metric)	2.0 x 1.25	Higher capacitance values	Used for **bulk decoupling away from the FPGA**

Package Sizes for Decoupling Under a BGA FPGA

Positioned Directly Beneath the BGA (Within the Via Field)

Employ 0201 or 0402 MLCCs placed in a dense grid layout under the BGA to facilitate effective decoupling of the core voltage.
•
Maintain a distance of less than 2mm between the capacitors and FPGA vias to achieve optimal transient response.

Just Outside the BGA Field

Utilize higher capacitance values (for example, 1µF in 0603)

Symmetrically position capacitors around the FPGA to promote balanced power distribution.
•**Adopt wider traces or direct power plane vias** for efficient connectivity.

Bulk Decoupling (Further Away)

0805, 1206, or 1210 10µF – 100µF MLCCs

Helps stabilize DC voltage and mitigates droop

Offers energy storage for low-frequency transients

Position bulk capacitors close to the power regulator inputs or **on a nearby PCB layer**.

•**Refrain from placing large capacitors directly beneath the BGA** because of space limitations.

Factors to Take into Account for Capacitor Package Sizes Continued…

Mitigating Assembly Challenges

0201 capacitors are more challenging to assemble and modify, so opt for **0402 when feasible**, unless ultra-low inductance is a necessity.

Utilise **X7R dielectric capacitors** for better stability across temperature and voltage ranges, and steer clear of X5R for aerospace applications.

Routing for Low Inductance

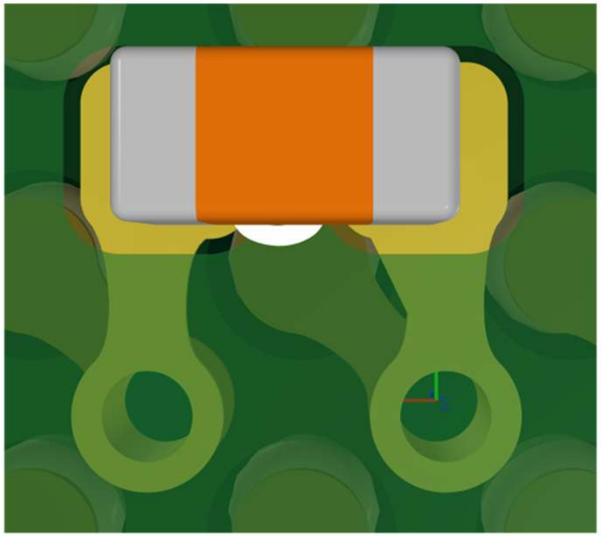
Implement via-in-pad (VIP) for enhanced decoupling efficiency (if fabrication methods and budget permit).

Minimise long traces—position capacitors **as close as possible to the FPGA power pins**.

High-Current Applications

In cases where the FPGA experiences **high-current transients (such as DDR and SERDES)**, it is advisable to utilize a combination of **0201, 0402, and 0603 capacitors** to effectively address a broad frequency spectrum.

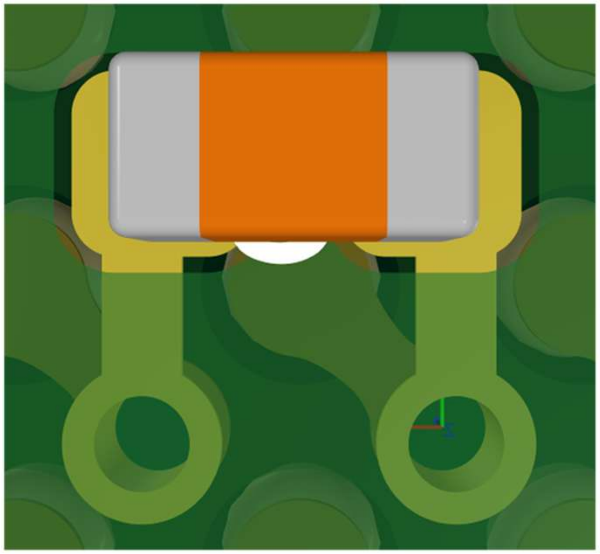
Advanced Topics Tear dropping Capacitors



Capacitor tear dropped pads, improved performance lower inductance, higher reliability connection

This is a typical 0402 capacitor positioned between P3V3 and 0V using a pair.

Key takeaway: consider the connections of tear-drop components, not just the vias!



Capacitor **NOT** tear dropped pads, standard performance no improvement in minimising inductance or improving connection reliability.